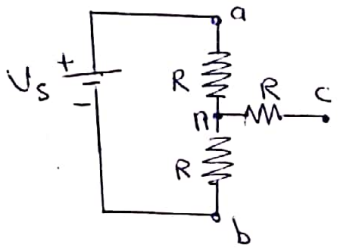
(a) 120° conduction

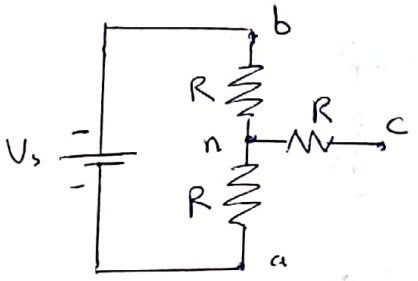
The waveforms at 120° conduction are shown in figure (3-2b). As a result, at any instant only two switches conduct. These waveforms are for resistive load. A 60° dead time exist between two series switches conducting, thereby providing a safety margin against simultaneous conducting of the two series devices across the dc supply rail. The dermination of the line & neutral voltages for balanced resistive load is shown in figure (3-3) below



$V_{ab} = V_s$

$V_{an} = \frac{V_s}{2}$

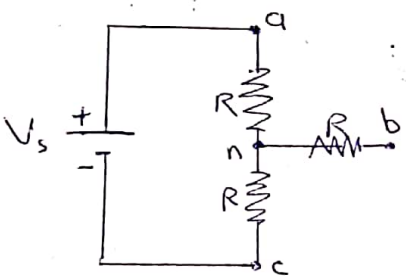
$0 \leq \omega t \leq \pi/3$



$V_{ab} = -V_s$

$V_{an} = \frac{-V_s}{2}$

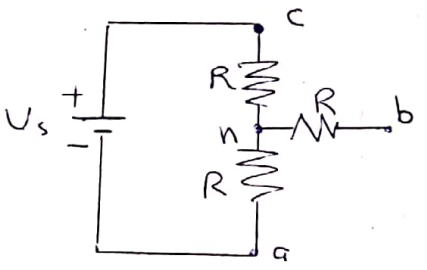
$\pi \leq \omega t \leq 4\pi/3$



$V_{ab} = \frac{V_s}{2}$

$V_{an} = \frac{V_s}{2}$

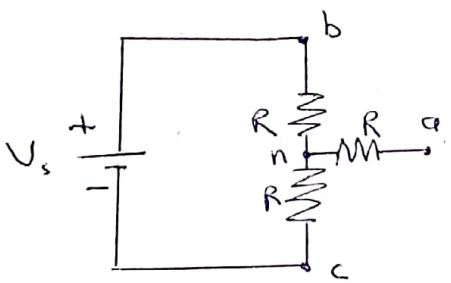
$\pi/3 \leq \omega t \leq 2\pi/3$



$V_{ab} = -\frac{V_s}{2}$

$V_{an} = -\frac{V_s}{2}$

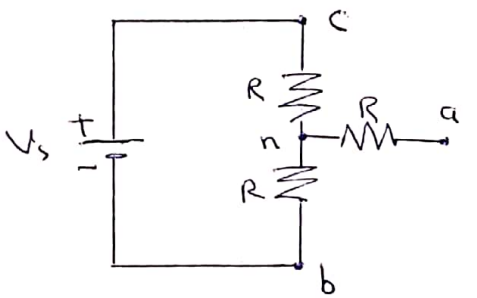
$4\pi/3 \leq \omega t \leq 5\pi/3$



$V_{ab} = -\frac{V_s}{2}$

$V_{an} = 0$

$2\pi/3 \leq \omega t \leq \pi$



$V_{ab} = \frac{V_s}{2}$

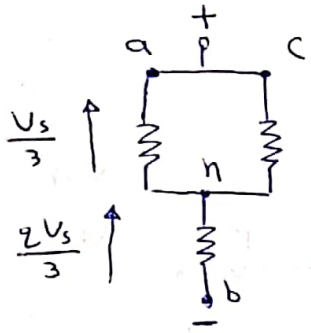
$V_{an} = 0$

$5\pi/3 \leq \omega t \leq 2\pi$

Figure (3-3)

(b) 180° conduction

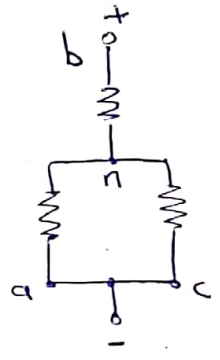
Figure (3.2c) shows inverter bridge quasi-square output voltage waveforms for a 180° switch conduction pattern. Each switch conducts for 180°, such that no two switches across the voltage rail conducts simultaneously. The determination of the voltage waveforms for balanced resistive load and 180° conduction are shown in figure (3.4) below.



$V_{ab} = V_s$

$V_{an} = \frac{V_s}{3}$

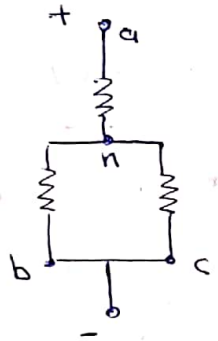
$0 \leq \omega t \leq \pi/3$



$V_{ab} = -V_s$

$V_{an} = -\frac{V_s}{3}$

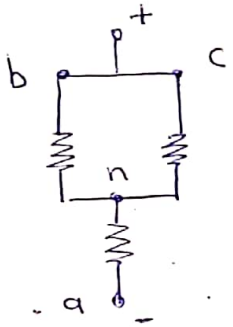
$\pi \leq \omega t \leq 4\pi/3$



$V_{ab} = V_s$

$V_{an} = \frac{2V_s}{3}$

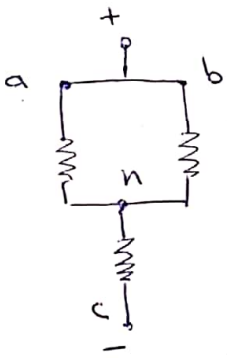
$\pi/3 \leq \omega t \leq 2\pi/3$



$V_{ab} = -V_s$

$V_{an} = -\frac{2V_s}{3}$

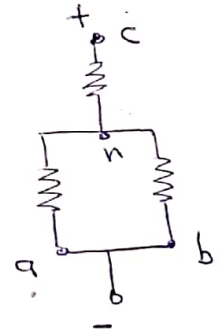
$4\pi/3 \leq \omega t \leq 5\pi/3$



$V_{ab} = 0$

$V_{an} = \frac{V_s}{3}$

$2\pi/3 \leq \omega t \leq \pi$



$V_{ab} = 0$

$V_{an} = -\frac{V_s}{3}$

$5\pi/3 \leq \omega t \leq 2\pi$

Figure (3.4)

(c) 180° conduction with inductive load *

When the load supplied by the inverter contains inductance, then the current in each arm of the load will be delayed to its voltage as shown in figure (3.5)

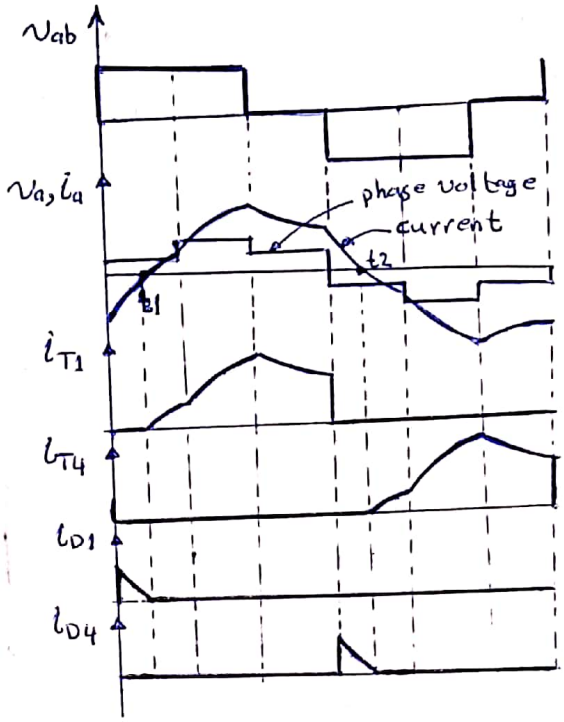


Figure (3.5) Waveforms for 180° firing with an inductive load.

When thyristor T1 is fired, thyristor T4 is turned off but, because the load current cannot reverse, the only path for this current is through D1. Hence the load phase is connected to the positive end of the d.c. source but until the load current reverses at t1, thyristor T1 will not take up conduction. Similar arguments apply in the reverse half cycle at t2.

* Reference (Lander P190-193)