**CPU BASICS**

A typical CPU has three major components:

 1- register set,

 2- arithmetic logic unit (ALU),

 3- control unit (CU).

 The figure below shows the internal structure of the CPU .

The CPU fetches instructions from memory, reads and writes data from and to memory, and transfers data from and to input/output devices.



**Instruction execution cycle:**

1- fetch: fetching next instruction( using PC) from memory into IR.

2-decode:decoding the instruction.

3- execute: executing the instruction.

 **REGISTER SET:**

• The register set differs from one computer architecture to another. It is usually a combination of general-purpose and special purpose registers

• *General-purpose registers* can be used for multiple purposes and assigned to a variety of functions by the programmer.

• *Special-purpose registers* are restricted to only specific functions.

 **Memory Access Registers:**

Two registers are essential in memory write and read operations: the memory data register (**MDR**) and memory address register (**MAR**). The MDR and MAR are used exclusively by the CPU and are not directly accessible to programmers.

In order to perform a **write** operation into a specified memory location, the MDR and MAR are used as follows:

**1.** The word to be stored into the memory location is first loaded by the CPU into **MDR**.

**2.** The address of the location into which the word is to be stored is loaded by the CPU into a **MAR**.

**3.** A write signal is issued by the CPU.

 Similarly, to perform a memory **read** operation, the MDR and MAR are used as follows:

**1.** The address of the location from which the word is to be read is loaded into the **MAR.**

**2.** A read signal is issued by the CPU.

**3.** The required word will be loaded by the memory into the **MDR** ready for use by the CPU.

**Instruction Fetching Registers:**

Two main registers are involved in fetching an instruction for execution: the program counter (**PC**) and the instruction register (**IR**). The PC is the register that contains the address of the next instruction to be fetched. The fetched instruction is loaded in the IR .

 **Condition Register:** Program status word (**PSW**) register contains bits that are set by the CPU to indicate the current status of an executing program. These indicators are typically for arithmetic operations, interrupts,…etc.

 **Special-Purpose Address Registers:**

• In index addressing, the **index register**  holds an address displacement which when added to a constant, the address of the operand is obtained.

• A **segment register** holds the address of the base of the segment.

• A specific register, called the **stack pointer (SP**), is used to indicate the stack location that can be addressed. In the stack push operation, the SP is incremented and in pop operation the SP is decremented.