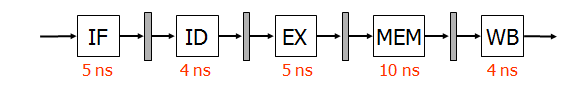
**Pipelining**

*\* Pipelining* is an implementation technique used to build fast processors. It allows the execution of multiple instructions to overlap in time.

**Pipeline Stages**



The computer pipeline divide the instruction processing into stages. Each stage completes a part of an instruction and loads a new part in parallel.

We can divide the execution of an instruction into the following 5 “classic” stages:

**IF:** Instruction Fetch

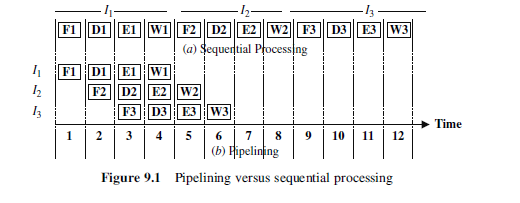
**ID:** Instruction Decode, register fetch

**EX:** Execution

**MEM:** Memory Access

**WB:** Register write Back

**Example:** Compute the time needed to process three instructions in four-stage pipelining versus sequential technique.



It is clear from the figure that the total time required to process three instructions (I1, I2, I3) is only **six** time units if four-stage pipelining is used as compared to **12** time units if sequential processing is used.

**Advantages/Disadvantages**

Advantages:

* More efficient use of processor
* Quicker time of execution of large number of instructions

Disadvantages:

* Pipelining involves adding hardware to the chip
* Inability to continuously run the pipeline at full speed because of pipeline hazards which disrupt the smooth execution of the pipeline.

**Pipeline Throughput and Latency:**

**Pipeline throughput**: instructions completed per second

**Pipeline latency**: how long does it take to execute single instruction in the pipeline.