Bipolar Junction Transistors

During the period 1904–1947, the vacuum tube was undoubtedly the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Walter H. Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories.

The advantages of this three terminal solid-state device over the tube were immediately obvious: It was smaller and lightweight; had no heater requirement or heater loss; had rugged construction; and was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. You will find that all amplifiers (devices that increase the voltage, current, or power level) will have at least three terminals with one controlling the flow between two other terminals.

TRANSISTOR CONSTRUCTION

The transistor is a three-layer semiconductor device consisting of either two $n$- and one $p$-type layers of material or two $p$- and one $n$-type layers of material. The former is called an $npn$ transistor, while the latter is called a $pnp$ transistor. Both are shown in Fig. 3.2 with the proper dc biasing. We will find in Chapter 4 that the dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped.

The outer layers have widths much greater than the sandwiched $p$- or $n$-type material. For the transistors shown in Fig. 3.2 the ratio of the total width to that of the center layer is $0.150/0.001 = 150:1$. 

![Diagrams of npn and pnp transistors](image-url)
The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10:1 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of “free” carriers.

The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device. The Schottky diode of Chapter 20 is such a device.

**COMMON-BASE CONFIGURATION**

The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential.

**Alpha (α)**

In the dc mode the levels of $I_C$ and $I_E$ due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E}$$

where $I_C$ and $I_E$ are the levels of current at the point of operation.

**Alpha ac = delta $I_C$/delta $I_E$**

The ac alpha is formally called the common-base, short-circuit, amplification factor.
**EXAMPLE 3.1**  
(a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_C = 3$ mA and $V_{CB} = 10$ V.  
(b) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_C$ remains at 3 mA but $V_{CB}$ is reduced to 2 V.  
(c) Using the characteristics of Figs. 3.7 and 3.8, determine $V_{BE}$ if $I_C = 4$ mA and $V_{CB} = 20$ V.

**Solution**  
(a) The characteristics clearly indicate that $I_C = I_E = 3$ mA.  
(b) The effect of changing $V_{CB}$ is negligible and $I_C$ continues to be 3 mA.  
(c) From Fig. 3.8, $I_E = I_C = 4$ mA. On Fig. 3.7 the resulting level of $V_{BE}$ is about 0.74 V.

**Alpha ($\alpha$)**  
called alpha and defined by the following equation:

\[
\alpha_{dc} = \frac{I_C}{I_E}
\]

alpha typically extends from 0.90 to 0.998,

where $I_C$ and $I_E$ are the levels of current at the point of operation.

\[
I_C = \alpha I_E + I_{CBO}
\]  
(3.6)

For the characteristics of Fig. 3.8 when $I_E = 0$ mA, $I_C$ is therefore equal to $I_{CBO}$. but as mentioned earlier, the level of $I_{CBO}$ is usually so small that it is virtually undetectable on the graph of Fig. 3.8. In other words, when $I_E = 0$ mA on Fig. 3.8, $I_C$ also appears to be 0 mA for the range of $V_{CB}$ values.

\[
\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \bigg|_{V_{CB} \text{ constant}}
\]

The ac alpha is formally called the **common-base, short-circuit, amplification factor**, that a relatively small change in collector current is divided by the corresponding change in IE with the collector-to-base voltage held constant. For most situations the magnitudes of $\alpha_{ac}$ and $\alpha_{dc}$ are quite close.

**BIASING**

![Biasing diagram](image)

**TRANSISTOR AMPLIFYING ACTION**

For the common-base configuration the ac input resistance determined by the characteristics of Fig. 3.7 is quite small and typically varies from 10 to 100 ohm.
The output resistance as determined by the curves of Fig. 3.8 is quite high (the more horizontal the curves the higher the resistance) and typically varies from 50 k ohm to 1 M ohm (100 k ohm for the transistor of Fig. 3.12). The difference in resistance is due to the forward-biased junction at the input (base to emitter) and the reverse-biased junction at the output (base to collector). Using a common value of 20 ohm for the input resistance, we find that

\[
I = \frac{V}{R_I} = \frac{200 \text{ mV}}{20 \Omega} = 10 \text{ mA}
\]

If we assume for the moment that \( \alpha_{ac} = 1 \) \( (I_c = I_e) \),

\[
I_L = I_i = 10 \text{ mA}
\]

and

\[
V_L = I_L R
\]

\[
= (10 \text{ mA})(5 \text{ k}\Omega)
\]

\[
= 50 \text{ V}
\]

**Figure 3.12** Basic voltage amplification action of the common-base configuration.

The voltage amplification is

\[
A_v = \frac{V_L}{V_i} = \frac{50 \text{ V}}{200 \text{ mV}} = 250
\]

Typical values of voltage amplification for the common-base configuration vary from 50 to 300. The current amplification \( (I_c/I_E) \) is always less than 1 for the common-base configuration. This latter characteristic should be obvious since \( I_c = \alpha I_E \) and \( \alpha \) is always less than 1.

The basic amplifying action was produced by transferring a current \( I \) from a low-to a high-resistance circuit. The combination of the two terms in italics results in the label transistor; that is,

\[
\text{transfer + resistor} \rightarrow \text{transistor}
\]

**COMMON-EMITTER CONFIGURATION**

It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals), one for the input or base-emitter circuit and one for the output or collector-emitter circuit. Both are shown in Fig. 3.14.
Consider also that the curves of $I_B$ are not as horizontal as those obtained for $I_E$ in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for $I_B$ are nearly straight and equally spaced. In Fig. 3.14a this region exists to the right of the vertical dashed line $V_{CE_{Sat}}$ and above the curve for $I_B$ equal to zero. The region to the left of $V_{CE_{Sat}}$ is called the saturation region.

In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.
conclusion that for a transistor in the “on” or active region the base-to-emitter voltage is 0.7V. In this case the voltage is fixed for any level of base current.

The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.14 that $I_C$ is not equal to zero when $I_B$ is zero. For the common-base configuration, when the input current $I_E$ was equal to zero, the collector current was equal only to the reverse saturation current $I_CBO$, so that the curve $I_E = 0$ and the voltage axis were, for all practical purposes, one.

The reason for this difference in collector characteristics can be derived through the proper manipulation of Eqs. (3.3) and (3.6). That is,

Eq. (3.6):  $I_C = \alpha I_E + I_CBO$

Substitution gives  Eq. (3.3):  $I_C = \alpha(I_C + I_B) + I_CBO$

Rearranging yields

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_CBO}{1 - \alpha}$$

(3.8)

If we consider the case discussed above, where $I_B = 0 \, \text{A}$, and substitute a typical value of $\alpha$ such as 0.996, the resulting collector current is the following:

$$I_C = \frac{\alpha(0 \, \text{A})}{1 - \alpha} + \frac{I_CBO}{1 - 0.996}$$

$$= \frac{I_CBO}{0.004} = 250I_CBO$$

If $I_CBO$ were 1 $\mu$A, the resulting collector current with $I_B = 0 \, \text{A}$ would be 250(1 $\mu$A) = 0.25 mA, as reflected in the characteristics of Fig. 3.14.

For future reference, the collector current defined by the condition $I_B = 0 \, \mu\text{A}$ will be assigned the notation indicated by Eq. (3.9).

$$I_{CEO} = \frac{I_CBO}{1 - \alpha} |_{I_B = 0 \, \mu\text{A}}$$

(3.9)

In other words, the region below $I_B = 0 \, \mu\text{A}$ is to be avoided if an undistorted output signal is required.

When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region. The cutoff condition should ideally be $I_C = 0 \, \text{mA}$ for the chosen $V_{CE}$ voltage. Since $I_{CEO}$ is typically low in magnitude for silicon materials, cutoff will exist for switching purposes when $I_B = 0 \, \mu\text{A}$ or $I_C = I_{CEO}$ for silicon transistors only. For germanium transistors, however, cutoff for switching purposes will be defined as those conditions that exist when $I_C = I_{CEO}$. This condition can normally be obtained for germanium transistors by reverse-biasing the base-to-emitter junction a few tenths of a volt.
(a) Using the characteristics of Fig. 3.14, determine $I_C$ at $I_B = 30 \mu A$ and $V_{CE} = 10 \text{ V}$.
(b) Using the characteristics of Fig. 3.14, determine $I_C$ at $V_{BE} = 0.7 \text{ V}$ and $V_{CE} = 15 \text{ V}$.

Solution

(a) At the intersection of $I_B = 30 \mu A$ and $V_{CE} = 10 \text{ V}$, $I_C = 3.4 \text{ mA}$.
(b) Using Fig. 3.14b, $I_B = 20 \mu A$ at $V_{BE} = 0.7 \text{ V}$. From Fig. 3.14a we find that $I_C = 2.5 \text{ mA}$ at the intersection of $I_B = 20 \mu A$ and $V_{CE} = 15 \text{ V}$.

BETA:

\[
\beta_{dc} = \frac{I_C}{I_B}
\]

\[
\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE} = \text{constant}}
\]

The formal name for $\beta_{ac}$ is common-emitter, forward-current, amplification factor. Since the collector current is usually the output current for a common-emitter configuration and the base current the input current, the term amplification is included in the nomenclature above.

Although not exactly equal, the levels of $\beta_{ac}$ and $\beta_{dc}$ are usually reasonably close and are often used interchangeably. That is, if $\beta_{ac}$ is known, it is assumed to be about the same magnitude as $\beta_{dc}$, and vice versa. Keep in mind that in the same lot, the value of $\beta_{ac}$ will vary somewhat from one transistor to the next even though each transistor has the same number code. The variation may not be significant but for the majority of applications, it is certainly sufficient to validate the approximate approach above. Generally, the smaller the level of $I_{CEO}$, the closer the magnitude of the two betas. Since the trend is toward lower and lower levels of $I_{CEO}$, the validity of the foregoing approximation is further substantiated.
Figure 3.17 Determining $\beta_{ac}$ and $\beta_{dc}$ from the collector characteristics.

$$\beta_{ac} = \frac{I_{CE} - I_{C}}{I_{BE} - I_{B}} = \frac{3.2 \text{ mA} - 2.2 \text{ mA}}{30 \mu\text{A} - 20 \mu\text{A}} = \frac{1 \text{ mA}}{10 \mu\text{A}} = 100$$

The solution above reveals that for an ac input at the base, the collector current will be about 100 times the magnitude of the base current.

If we determine the dc beta at the Q-point:

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7 \text{ mA}}{25 \mu\text{A}} = 108$$

Figure 3.18 Characteristics in which $\beta_{ac}$ is the same everywhere and $\beta_{ac} = \beta_{dc}$. 
If the characteristics had the appearance of those appearing in Fig. 3.18, the level of $\beta_{ac}$ would be the same in every region of the characteristics. Note that the step in $I_B$ is fixed at 10 $\mu$A and the vertical spacing between curves is the same at every point in the characteristics—namely, 2 mA. Calculating the $\beta_{ac}$ at the $Q$-point indicated will result in

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{ce} = \text{constant}} = \frac{9 \text{ mA} - 7 \text{ mA}}{45 \mu\text{A} - 35 \mu\text{A}} = \frac{2 \text{ mA}}{10 \mu\text{A}} = 200$$

Determining the dc beta at the same $Q$-point will result in

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{8 \text{ mA}}{40 \mu\text{A}} = 200$$

A relationship can be developed between $\beta$ and $\alpha$ using the basic relationships introduced thus far. Using $\beta = I_C/I_B$ we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by $I_C$ will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\alpha = \frac{\beta}{\beta + 1} \quad (3.12a)$$

or

$$\beta = \frac{\alpha}{1 - \alpha} \quad (3.12b)$$

In addition, recall that

$$I_{CEO} = \frac{I_{CEO}}{1 - \alpha}$$

but using an equivalence of
The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

\[
\frac{1}{1 - \alpha} = \beta + 1
\]

derived from the above, we find that

\[
I_{CEO} = (\beta + 1)I_{CBO}
\]

or

\[
I_{CEO} \approx \beta I_{CBO}
\]

as indicated on Fig. 3.14a. Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

\[
I_C = \beta I_R
\]

and since

\[
I_K = I_C + I_B
\]

\[
= \beta I_B + I_B
\]

we have

\[
I_E = (\beta + 1)I_B
\]

Both of the equations above play a major role in the analysis in Chapter 4.

### 3.7 COMMON-COLLECTOR CONFIGURATION

The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

**Figure 3.20** Notation and symbols used with the common-collector configuration: (a) pnp transistor; (b) npn transistor.
A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration.

From a design viewpoint, there is no need for a set of common-collector characteristics to choose the parameters of the circuit of Fig. 3.21. It can be designed using the common-emitter characteristics of Section 3.6. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration, the output characteristics are a plot of $I_E$ versus $V_{EC}$ for a range of values of $I_B$. The input current, therefore, is the same for both the common-emitter and common-collector characteristics.

The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of $I_C$ of the common-emitter characteristics if $I_C$ is replaced by $I_E$ for the common-collector characteristics (since $\alpha = 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.
Figure 3.14 Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.
Figure 3.7: Input or driving point characteristics for a common-base silicon transistor amplifier.

Figure 3.8: Output or collector characteristics for a common-base transistor amplifier.
The analysis or design of a transistor amplifier requires a knowledge of both the dc and ac response of the system.

**V_{BE} = 0.7 \text{ V}**

**I_{E} = (\beta + 1)I_{B} \equiv I_{C}**

**I_{C} = \beta I_{B}**

**OPERATING POINT**

*quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive.

The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current \( I \) and a vertical line at the maximum collector-to-emitter voltage \( V_{C\text{E}_{\text{max}}} \). The maximum power constraint is defined by the curve \( P_{\text{emax}} \) in the same figure.

If no bias were used, the device would initially be completely off, resulting in a *Q*-point at \( A \)—namely, zero current through the device (and zero voltage across it). The effect of temperature must also be taken into account.
Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network.

*stability factor*, $S$, which indicates the degree of change in operating point due to a temperature variation.

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base–emitter junction *must* be forward-biased (*p*-region voltage more positive), with a resulting forward-bias voltage of about 0.6 to 0.7 V.
2. The base–collector junction *must* be reverse-biased (*n*-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

[Note that for forward bias the voltage across the *p*-n junction is *p*-positive, while for reverse bias it is opposite (reverse) with *n*-positive.

**FIXED-BIAS CIRCUIT**

The fixed-bias circuit of Fig. 4.2 provides a relatively straightforward and simple introduction to transistor dc bias analysis.

the base–emitter circuit loop applying Kirchhoff’s voltage equation

\[
+ V_{CC} - I_B R_B - V_{BE} = 0
\]

\[
I_B = \frac{V_{CC} - V_{BE}}{R_B}
\]

**Collector–Emitter Loop**

\[
V_{CE} + I_C R_C - V_{CC} = 0
\]

\[
V_{CE} = V_{CC} - I_C R_C
\]
Collector–Emitter Loop

It is interesting to note that since the base current is controlled by the level of \( R_B \) and \( I_C \) is related to \( I_B \) by a constant \( B \), the magnitude of \( I_C \) is not a function of the resistance \( R_C \). Change \( R_C \) to any level and it will not affect the level of \( I_B \) or \( I_C \) as long as we remain in the active region of the device.

\[
I_C = \beta I_B
\]

Applying Kirchhoff’s voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 will result in the following:

\[
\begin{align*}
V_{CE} + I_C R_C - V_{CC} &= 0 \\
V_{CE} &= V_{CC} - I_C R_C \\
V_{CE} &= V_C - V_E \\
V_{CE} &= V_C \\
V_{BE} &= V_B - V_E \\
V_{BE} &= V_R
\end{align*}
\]

Ex:

Determine the following for the fixed-bias configuration of Fig. 4.7.
(a) \( I_{B_0} \) and \( I_{C_0} \).
(b) \( V_{CE_0} \).
(c) \( V_B \) and \( V_C \).
(d) \( V_{RC} \).
Transistor Saturation
The term saturation is applied to any system where levels have reached their maximum values.
Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted.

\[ R_{CE} = \frac{V_{CE}}{I_{C}} = \frac{0 \text{ V}}{I_{C_{sat}}} = 0 \text{ } \Omega \]

\[ I_{C_{sat}} = \frac{V_{CC}}{R_{C}} \]
Load-Line Analysis
called the load line since it is defined by the load resistor $R_c$. If the level of $I_B$ is changed by varying the value of $R_B$ the $Q$-point moves up or down the load line as shown in Fig. 4.13.

down the load line as shown in Fig. 4.13. If $V_{CC}$ is held fixed and $R_C$ changed, the load line will shift as shown in Fig. 4.14. If $I_B$ is held fixed, the $Q$-point will move as shown in the same figure. If $R_C$ is fixed and $V_{CC}$ varied, the load line shifts as shown in Fig. 4.15.

**EXAMPLE 4.3** Given the load line of Fig. 4.16 and the defined $Q$-point, determine the required values of $V_{CC}$, $R_C$, and $R_B$ for a fixed-bias configuration.
4.4 EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.

**Solution**

From Fig. 4.16,

\[
V_{CE} = V_{CC} = 20 \text{ V at } I_C = 0 \text{ mA}
\]

\[
I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}
\]

and

\[
R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k} \Omega
\]

\[
I_B = \frac{V_{CC} - V_{BE}}{R_B}
\]

and

\[
R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25 \mu\text{A}} = 772 \text{ k} \Omega
\]

---

**Base–Emitter Loop**

Kirchhoff's voltage law around the indicated loop in the clockwise direction

\[
+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0
\]

(4.15)
\[ I_E = (\beta + 1)I_B \]

Substituting for \( I_E \) in Eq. (4.15) will result in

\[ V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0 \]

Grouping terms will then provide the following:

\[ -(I_B R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0 \]

Multiplying through by \(-1\) we have

\[ I_B (R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0 \]

with

\[ I_B (R_B + (\beta + 1)R_E) = V_{CC} - V_{BE} \]

and solving for \( I_B \) gives

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \]

(4.17)

**Figure 4.18** Base–emitter loop.

**Figure 4.19** Network derived from Eq. (4.17).

**Figure 4.20** Reflected impedance level of \( R_b \).

The equation obtained above. Note that aside from the base-to-emitter voltage \( V_{BE} \), the resistor \( R_E \) is reflected back to the input base circuit by a factor \((\beta + 1)\). In other words, the emitter resistor, which is part of the collector–emitter loop, “appears as” \((\beta + 1)R_E\) in the base–emitter loop. Since \( \beta \) is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.20,

\[ R_i = (\beta + 1)R_E \]

(4.18)

**Collector–Emitter Loop**

Writing Kirchhoff’s voltage law

\[ +I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]

Substituting \( I_E = I_C \) and grouping terms gives

\[ V_{CE} - V_{CC} + I_C (R_C + R_E) = 0 \]

and

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

(4.19)

The single-subscript voltage \( V_E \) is the voltage from emitter to ground and is determined by

\[ V_E = I_E R_E \]

(4.20)

**Figure 4.21** Collector–emitter loop.
while the voltage from collector to ground can be determined from

\[ V_{CE} = V_C - V_E \]

and

\[ V_C = V_{CE} + V_E \]

(4.21)

or

\[ V_C = V_{CC} - I_c R_C \]

(4.22)

The voltage at the base with respect to ground can be determined from

\[ V_B = V_{CC} - I_B R_B \]

(4.23)

or

\[ V_B = V_{BE} + V_E \]

(4.24)

For the emitter bias network of Fig. 4.22, determine:

(a) \( I_B \)
(b) \( I_C \)
(c) \( V_{CE} \)
(d) \( V_C \)
(e) \( V_E \)
(f) \( V_B \)
(g) \( V_{BC} \)

**EXAMPLE 4.4**

![Emitter-stabilized bias circuit for Example 4.4.](image)

**Solution**

(a) Eq. (4.17): 
\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)} \]
\[ = \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \text{ \mu A} \]

(b) \( I_C = \beta I_B \)
\[ = (50)(40.1 \text{ \mu A}) \]
\[ = 2.01 \text{ mA} \]

(c) Eq. (4.19): 
\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]
\[ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V} \]
\[ = 13.97 \text{ V} \]

(d) \( V_C = V_{CC} - I_C R_C \)
\[ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V} \]
\[ = 15.98 \text{ V} \]

(e) \( V_E = V_C - V_{CE} \)
\[ = 15.98 \text{ V} - 13.97 \text{ V} \]
\[ = 2.01 \text{ V} \]

or \( V_E = I_E R_E \equiv I_C R_E \)
\[ = (2.01 \text{ mA})(1 \text{ k}\Omega) \]
\[ = 2.01 \text{ V} \]

(f) \( V_B = V_{BE} + V_E \)
\[ = 0.7 \text{ V} + 2.01 \text{ V} \]
\[ = 2.71 \text{ V} \]

(g) \( V_{BC} = V_B - V_C \)
\[ = 2.71 \text{ V} - 15.98 \text{ V} \]
\[ = -13.27 \text{ V} \] (reverse-biased as required)
EXAMPLE 4.5

Prepare a table and compare the bias voltage and currents of the circuits of Figs. 4.7 and Fig. 4.22 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in $I_C$ and $V_{CE}$ for the same increase in $\beta$.

Solution

Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

<table>
<thead>
<tr>
<th>$\beta$</th>
<th>$I_R$ ((\mu A))</th>
<th>$I_C$ (mA)</th>
<th>$V_{CE}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>47.08</td>
<td>2.35</td>
<td>6.83</td>
</tr>
<tr>
<td>100</td>
<td>47.08</td>
<td>4.71</td>
<td>1.64</td>
</tr>
</tbody>
</table>

The BJT collector current is seen to change by 100% due to the 100% change in the value of $\beta$. $I_R$ is the same and $V_{CE}$ decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

<table>
<thead>
<tr>
<th>$\beta$</th>
<th>$I_R$ ((\mu A))</th>
<th>$I_C$ (mA)</th>
<th>$V_{CE}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>40.1</td>
<td>2.04</td>
<td>13.97</td>
</tr>
<tr>
<td>100</td>
<td>36.3</td>
<td>3.63</td>
<td>9.11</td>
</tr>
</tbody>
</table>

Now the BJT collector current increases by about 81% due to the 100% increase in $\beta$. Notice that $I_R$ decreased, helping maintain the value of $I_C$—or at least reducing the overall change in $I_C$ due to the change in $\beta$. The change in $V_{CE}$ has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 4.7 for the same change in $\beta$.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$  \hspace{1cm} (4.25)

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

\[\text{Figure 4.23 Determining } I_{C_{sat}} \text{ for the emitter-stabilized bias circuit} \]
EXAMPLE 4.6  Determine the saturation current for the network of Example 4.4.

Solution

\[ I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \]

\[ = \frac{20 \text{ V}}{2 \text{ k}\Omega + 1 \text{ k}\Omega} = \frac{20 \text{ V}}{3 \text{ k}\Omega} \]

\[ = 6.67 \text{ mA} \]

which is about twice the level of \( I_{C_{o}} \) for Example 4.4.
Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of $I_B$ as determined by Eq. (4.17) defines the level of $I_B$ on the characteristics of Fig. 4.24 (denoted $I_{Bq}$).

![Figure 4.24 Load line for the emitter-bias configuration.](image)

The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0$ mA gives

$$V_{CE} = V_{CC} igg|_{I_C=0 \text{ mA}}$$  \hspace{1cm} (4.26)

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$I_C = \frac{V_{CC}}{R_C + R_E} \bigg|_{V_{CE}=0 \text{ V}}$$  \hspace{1cm} (4.27)

as shown in Fig. 4.24. Different levels of $I_{Bq}$ will, of course, move the $Q$-point up or down the load line.

4.5 VOLTAGE-DIVIDER BIAS

In the previous bias configurations the bias current $I_{Cq}$ and voltage $V_{CEq}$ were a function of the current gain ($\beta$) of the transistor. However, since $\beta$ is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in

![Figure 4.25 Voltage-divider bias configuration.](image)  \hspace{1cm} ![Figure 4.26 Defining the Q-point for the voltage-divider bias configuration.](image)
fact, independent of the transistor beta. The voltage-divider bias configuration of Fig. 4.25 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of $I_{C_{Q}}$ and $V_{CE_{Q}}$ can be almost totally independent of beta. Recall from previous discussions that a $Q$-point is defined by a fixed level of $I_{C_{Q}}$ and $V_{CE_{Q}}$ as shown in Fig. 4.26. The level of $I_{BE}$ will change with the change in beta, but the operating point on the characteristics defined by $I_{C_{Q}}$ and $V_{CE_{Q}}$ can remain fixed if the proper circuit parameters are employed.

As noted above, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the exact method that can be applied to any voltage-divider configuration. The second is referred to as the approximate method and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

**Exact Analysis**

The input side of the network of Fig. 4.25 can be redrawn as shown in Fig. 4.27 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

![Figure 4.27](image)

**Figure 4.27** Redrawing the input side of the network of Fig. 4.25.

$R_{Th}$: The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.28.

$$ R_{Th} = R_1 || R_2 $$ (4.28)

$E_{Th}$: The voltage source $V_{CC}$ is returned to the network and the open-circuit Thévenin voltage of Fig. 4.29 determined as follows:

Applying the voltage-divider rule:

$$ E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} $$ (4.29)

![Figure 4.28](image)

**Figure 4.28** Determining $R_{Th}$.

The Thévenin network is then redrawn as shown in Fig. 4.30, and $I_{BO}$ can be determined by first applying Kirchhoff’s voltage law in the clockwise direction for the loop indicated:

$$ E_{Th} - I_{B} R_{Th} - V_{BE} - I_{E} R_{E} = 0 $$

Substituting $I_{E} = (\beta + 1)I_{B}$ and solving for $I_{B}$ yields

$$ I_{B} = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_{E}} $$ (4.30)

![Figure 4.29](image)

**Figure 4.29** Determining $E_{Th}$. 

$E_{Th}$.
Although Eq. (4.30) initially appears different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by \((\beta + 1)\)—certainly very similar to Eq. (4.17).

Once \(I_B\) is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

\[
V_{CE} = V_{CC} - I_C(R_C + R_E)
\]  

which is exactly the same as Eq. (4.19). The remaining equations for \(V_E, V_C,\) and \(V_B\) are also the same as obtained for the emitter-bias configuration.

Determine the dc bias voltage \(V_{CE}\) and the current \(I_C\) for the voltage-divider configuration of Fig. 4.31.

**EXAMPLE 4.7**

Determine the dc bias voltage \(V_{CE}\) and the current \(I_C\) for the voltage-divider configuration of Fig. 4.31.
Solution

Eq. (4.28): \( R_{Th} = R_1 || R_2 \)

\[
= \frac{(39 \text{ k}\Omega)(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 3.55 \text{ k}\Omega
\]

Eq. (4.29): \( E_{Th} = \frac{R_2V_{CC}}{R_1 + R_2} \)

\[
= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2 \text{ V}
\]

Eq. (4.30): \( I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \)

\[
= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (141)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 211.5 \text{ k}\Omega}
\]

\( = 6.05 \mu\text{A} \)

\( I_C = \beta I_B \)

\( = (140)(6.05 \mu\text{A}) \)

\( = 0.85 \text{ mA} \)

Eq. (4.31): \( V_{CE} = V_{CC} - I_C(R_C + R_E) \)

\[
= 22 \text{ V} - (0.85 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega)
\]

\( = 22 \text{ V} - 9.78 \text{ V} \)

\( = 12.22 \text{ V} \)

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.32. The resistance \( R_i \) is the equivalent resistance between base and ground for the transistor with an emitter resistor \( R_E \). Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by \( R_i = (\beta + 1)R_E \). If \( R_i \) is much larger than the resistance \( R_2 \), the current \( I_B \) will be much smaller than \( I_2 \) (current always seeks the path of least resistance) and \( I_2 \) will be approximately equal to \( I_1 \). If we accept the approximation that \( I_B \) is essentially zero amperes compared to \( I_1 \) or \( I_2 \), then \( I_1 = I_2 \) and \( R_1 \) and \( R_2 \) can be considered series ele-
ments. The voltage across $R_2$, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$  \hspace{1cm} (4.32)

Since $R_1 = (\beta + 1)R_E \approx \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \gg 10 R_2$$  \hspace{1cm} (4.33)

In other words, if $\beta$ times the value of $R_E$ is at least 10 times the value of $R_2$, the approximate approach can be applied with a high degree of accuracy.

Once $V_B$ is determined, the level of $V_E$ can be calculated from

$$V_E = V_B - V_{BE}$$  \hspace{1cm} (4.34)

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$  \hspace{1cm} (4.35)

and

$$I_{CQ} \equiv I_E$$  \hspace{1cm} (4.36)

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but since $I_E \equiv I_C$,

$$V_{CE_0} = V_{CC} - I_C (R_C + R_E)$$ \hspace{1cm} (4.37)

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that $\beta$ does not appear and $I_B$ was not calculated. The $Q$-point (as determined by $I_{CQ}$ and $V_{CE_0}$) is therefore independent of the value of $\beta$. 

**Figure 4.32** Partial-bias circuit for calculating the approximate base voltage $V_B$. 


Repeat the analysis of Fig. 4.31 using the approximate technique, and compare solutions for $I_{C_{o}}$ and $V_{CE_{o}}$.

**Solution**

Testing:

$$\beta R_e \approx 10R_2$$

$$(140)(1.5 \text{k}\Omega) \approx 10(3.9 \text{k}\Omega)$$

$$210 \text{k}\Omega \approx 39 \text{k}\Omega \text{ (satisfied)}$$

**Eq. (4.32):**

$$V_B = \frac{R_2V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9 \text{k}\Omega)(22 \text{V})}{39 \text{k}\Omega + 3.9 \text{k}\Omega}$$

$$= 2 \text{V}$$

Note that the level of $V_B$ is the same as $E_{Th}$ determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of $R_{Th}$ in the exact analysis that separates $E_{Th}$ and $V_B$.

**Eq. (4.34):**

$$V_E = V_B - V_{BE}$$

$$= 2 \text{V} - 0.7 \text{V}$$

$$= 1.3 \text{V}$$

$$I_{C_{o}} = I_E = \frac{V_E}{R_E} = \frac{1.3 \text{V}}{1.5 \text{k}\Omega} = 0.867 \text{mA}$$

compared to 0.85 mA with the exact analysis. Finally,

$$V_{CE_{o}} = V_{CC} - I_c(R_C + R_E)$$

$$= 22 \text{V} - (0.867 \text{mA})(10 \text{k}\Omega + 1.5 \text{k}\Omega)$$

$$= 22 \text{V} - 9.97 \text{V}$$

$$= 12.03 \text{V}$$

versus 12.22 V obtained in Example 4.7.

The results for $I_{C_{o}}$ and $V_{CE_{o}}$ are certainly close, and considering the actual variation in parameter values one can certainly be considered as accurate as the other. The larger the level of $R_e$ compared to $R_2$, the closer the approximate to the exact solution. Example 4.10 will compare solutions at a level well below the condition established by Eq. (4.33).
Determine the levels of $I_{C_q}$ and $V_{CE_q}$ for the voltage-divider configuration of Fig. 4.33 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) will not be satisfied but the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

![Figure 4.33 Voltage-divider configuration for Example 4.10.](image)

**Solution**

**Exact Analysis**

Eq. (4.33): \[ \beta R_E \geq 10R_2 \]

\[ (50)(1.2 \, \text{k}\Omega) \geq 10(22 \, \text{k}\Omega) \]

\[ 60 \, \text{k}\Omega \not\geq 220 \, \text{k}\Omega \] *(not satisfied)*

\[ R_{TH} = R_1 || R_2 = 82 \, \text{k}\Omega || 22 \, \text{k}\Omega = 17.35 \, \text{k}\Omega \]

\[ E_{TH} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22 \, \text{k}\Omega(18 \, \text{V})}{82 \, \text{k}\Omega + 22 \, \text{k}\Omega} = 3.81 \, \text{V} \]

\[ I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} = \frac{3.81 \, \text{V} - 0.7 \, \text{V}}{17.35 \, \text{k}\Omega + (51)(1.2 \, \text{k}\Omega)} = \frac{3.11 \, \text{V}}{78.55 \, \text{k}\Omega} \]

\[ = 39.6 \, \mu\text{A} \]

\[ I_{C_q} = \beta I_B = (50)(39.6 \, \mu\text{A}) = 1.98 \, \text{mA} \]

\[ V_{CE_q} = V_{CC} - I_C(R_C + R_E) \]

\[ = 18 \, \text{V} - (1.98 \, \text{mA})(5.6 \, \text{k}\Omega + 1.2 \, \text{k}\Omega) \]

\[ = 4.54 \, \text{V} \]

**Approximate Analysis**

\[ V_B = E_{TH} = 3.81 \, \text{V} \]

\[ V_E = V_B - V_{BE} = 3.81 \, \text{V} - 0.7 \, \text{V} = 3.11 \, \text{V} \]

\[ I_{C_q} \approx I_E = \frac{V_E}{R_E} = \frac{3.11 \, \text{V}}{1.2 \, \text{k}\Omega} = 2.59 \, \text{mA} \]
\[ V_{CEq} = V_{CC} - I_c(R_C + R_E) \]

\[ = 18 \text{ V} - (2.59 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega) \]

\[ = 3.88 \text{ V} \]

Tabulating the results, we have:

<table>
<thead>
<tr>
<th>( I_{Cq} ) (mA)</th>
<th>( V_{CEq} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exact</td>
<td>1.98</td>
</tr>
<tr>
<td>Approximate</td>
<td>2.59</td>
</tr>
<tr>
<td></td>
<td>4.54</td>
</tr>
<tr>
<td></td>
<td>3.88</td>
</tr>
</tbody>
</table>

The results reveal the difference between exact and approximate solutions. \( I_{Cq} \) is about 30% greater with the approximate solution, while \( V_{CEq} \) is about 10% less. The results are notably different in magnitude, but even though \( \beta R_E \) is only about three times larger than \( R_Z \), the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

**Transistor Saturation**

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when \( V_{CE} \) is set to zero volts on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

\[ I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E} \]  \hspace{1cm} (4.38)

**Load-Line Analysis**

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.24, with

\[ I_c = \left. \frac{V_{CC}}{R_C + R_E} \right|_{V_{CE}=0 \text{ V}} \]  \hspace{1cm} (4.39)

and

\[ V_{CE} = V_{CC} \bigg| \hspace{0.1cm} I_C=0 \text{ mA} \]  \hspace{1cm} (4.40)

The level of \( I_C \) is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.
4.6 DC BIAS WITH VOLTAGE FEEDBACK

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.34. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop with the results applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.35 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff’s voltage law around the indicated loop in the clockwise direction will result in

\[ V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0 \]

\[ V_{CC} - I_C R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0 \]

Gathering terms, we have

\[ V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0 \]

and solving for \( I_B \)

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)} \quad (4.41) \]

The result is quite interesting in that the format is very similar to equations for \( I_B \) obtained for earlier configurations. The numerator is again the difference of available voltage levels, while the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance \( R_C \) back to the input circuit, much like the reflection of \( R_E \).

In general, the equation for \( I_B \) has had the following format:
\[ I_B = \frac{V'}{R_B + \beta R'} \]

with the absence of \( R' \) for the fixed-bias configuration, \( R' = R_E \) for the emitter-bias setup (with \( (\beta + 1) \equiv \beta \)), and \( R' = R_C + R_E \) for the collector-feedback arrangement. The voltage \( V' \) is the difference between two voltage levels. Since \( I_C = \beta I_B \),

\[ I_{C_o} = \frac{\beta V'}{R_B + \beta R'} \]

In general, the larger \( \beta R' \) is compared to \( R_B \), the less the sensitivity of \( I_{C_o} \) to variations in beta. Obviously, if \( \beta R' \gg R_B \) and \( R_B + \beta R' \approx \beta R' \), then

\[ I_{C_o} = \frac{\beta V'}{R_B + \beta R'} \approx \frac{\beta V'}{\beta R'} = \frac{V'}{R'} \]

and \( I_{C_o} \) is independent of the value of beta. Since \( R' \) is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, \( R' \) is zero ohms for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

**Collector–Emitter Loop**

The collector–emitter loop for the network of Fig. 4.34 is provided in Fig. 4.36. Applying Kirchhoff’s voltage law around the indicated loop in the clockwise direction will result in

\[ I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]

Since \( I'_C \equiv I_C \) and \( I_E \equiv I_C \), we have

\[ I_C (R_C + R_E) + V_{CE} - V_{CC} = 0 \]

and

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]  \hspace{1cm} (4.42)

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.
EXAMPLE 4.11  

Determine the quiescent levels of $I_{CQ}$ and $V_{CEQ}$ for the network of Fig. 4.37.

Solution

Eq. (4.41):  
\[
I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}
\]
\[
= \frac{10 \, \text{V} - 0.7 \, \text{V}}{250 \, \text{k}\Omega + (90)(4.7 \, \text{k}\Omega + 1.2 \, \text{k}\Omega)}
\]
\[
= \frac{9.3 \, \text{V}}{250 \, \text{k}\Omega + 531 \, \text{k}\Omega} = \frac{9.3 \, \text{V}}{781 \, \text{k}\Omega}
\]
\[
= 11.91 \, \mu\text{A}
\]

$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$
\[
= 10 \, \text{V} - (1.07 \, \text{mA})(4.7 \, \text{k}\Omega + 1.2 \, \text{k}\Omega)
\]
\[
= 10 \, \text{V} - 6.31 \, \text{V}
\]
\[
= 3.69 \, \text{V}
\]

Figure 4.37  

Network for Example 4.11.

Determine the dc level of $I_B$ and $V_C$ for the network of Fig. 4.38.

Solution

In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence and $R_B = R_1 + R_2$.

Solving for $I_B$ gives

\[
I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}
\]
\[
= \frac{18 \, \text{V} - 0.7 \, \text{V}}{(91 \, \text{k}\Omega + 110 \, \text{k}\Omega) + (75)(3.3 \, \text{k}\Omega + 0.51 \, \text{k}\Omega)}
\]
\[
= \frac{17.3 \, \text{V}}{201 \, \text{k}\Omega + 285.75 \, \text{k}\Omega} = \frac{17.3 \, \text{V}}{486.75 \, \text{k}\Omega}
\]
\[
= 35.5 \, \mu\text{A}
\]
\[ I_C = \beta I_B \]
\[ = (75)(35.5 \ \mu A) \]
\[ = 2.66 \ \text{mA} \]
\[ V_C = V_{CC} - I_C R_C \equiv V_{CC} - I_e R_C \]
\[ = 18 \ \text{V} - (2.66 \ \text{mA})(3.3 \ \text{k} \Omega) \]
\[ = 18 \ \text{V} - 8.78 \ \text{V} \]
\[ = 9.22 \ \text{V} \]

**Saturation Conditions**

Using the approximation \( I'_C = I_C \), the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

\[
I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.43}
\]

**Load-Line Analysis**

Continuing with the approximation \( I'_C = I_C \) will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of \( I_{B_{dc}} \) will be defined by the chosen bias configuration.

**Design of a Bias Circuit with an Emitter Feedback Resistor**

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.50. The supply voltage and operating point were selected from the manufacturer’s information on the transistor used in the amplifier.

![Figure 4.50 Emitter-stabilized bias circuit for design consideration.](image-url)
The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector-emitter loop has two unknown quantities present—the resistors \( R_C \) and \( R_E \). At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of voltage swing of the voltage from collector to emitter (to be noted when the ac response is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor \( R_E \) and the resistor \( R_C \) in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.49 using the criteria just introduced for the emitter voltage.

Determine the resistor values for the network of Fig. 4.50 for the indicated operating point and supply voltage.

**Example 4.22**

**Solution**

\[
V_E = \frac{1}{10} V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}
\]

\[
R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{2 \text{ V}}{2 \text{ mA}} = 1 \text{ k}\Omega
\]

\[
R_C = \frac{V_{RC}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 10 \text{ V} - 2 \text{ V}}{2 \text{ mA}} = \frac{8 \text{ V}}{2 \text{ mA}} = 4 \text{ k}\Omega
\]

\[
I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{150} = 13.33 \mu\text{A}
\]

\[
R_B = \frac{V_{RB}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V} - 2 \text{ V}}{13.33 \mu\text{A}} \approx 1.3 \text{ M}\Omega
\]

**Design of a Current-Gain-Stabilized (Beta-Independent) Circuit**

The circuit of Fig. 4.51 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage, \( V_E \), as in the previous design consideration, leads to a direct straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.
Determine the levels of $R_C$, $R_E$, $R_1$, and $R_2$ for the network of Fig. 4.51 for the operating point indicated.

**Solution**

\[
V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}
\]

\[
R_E = \frac{V_E}{I_E} = \frac{2 \text{ V}}{10 \text{ mA}} = 200 \Omega
\]

\[
R_C = \frac{V_{R_E}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 \text{ V} - 8 \text{ V} - 2 \text{ V}}{10 \text{ mA}} = \frac{10 \text{ V}}{10 \text{ mA}} = 1 \text{ k}\Omega
\]

\[
V_B = V_{BE} + V_E = 0.7 \text{ V} + 2 \text{ V} = 2.7 \text{ V}
\]

The equations for the calculation of the base resistors $R_1$ and $R_2$ will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns, $R_1$ and $R_2$. An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through $R_1$ and $R_2$ should be approximately equal and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

\[
R_2 = \frac{1}{10}BR_E
\]

and

\[
V_B = \frac{R_2}{R_1 + R_2}V_{CC}
\]

Substitution yields

\[
R_2 = \frac{1}{10}(80)(0.2 \text{ k}\Omega) = 1.6 \text{ k}\Omega
\]

\[
V_B = 2.7 \text{ V} = \frac{(1.6 \text{ k}\Omega)(20 \text{ V})}{R_1 + 1.6 \text{ k}\Omega}
\]

and

\[
2.7R_1 + 4.32 \text{ k}\Omega = 32 \text{ k}\Omega
\]

\[
2.7R_1 = 27.68 \text{ k}\Omega
\]

\[
R_1 = 10.25 \text{ k}\Omega \quad \text{(use 10 k}\Omega)\]