CHAPTER 9
8086/8088 Hardware Specifications

CHAPTER OBJECTIVES

Upon completion of this chapter, you will be able to:

1. Describe the function of each 8086 and 8088 pin.
2. Understand the microprocessor's DC characteristics and indicate its fan-out to common logic families.
3. Use the clock generator chip (8284A) to provide the clock for the microprocessor.
4. Connect buffers and latches to the buses.
5. Interpret the timing diagrams.
6. Describe wait states and connect the circuitry required to cause various numbers of waits.
7. Explain the difference between minimum and maximum mode operation.

The Pin-Out

Figure 9–1 illustrates the pin-outs of the 8086 and 8088 microprocessors. As a close comparison reveals, there is virtually no difference between these two microprocessors—both are packaged in 40-pin dual in-line packages (DIPs).

As mentioned in Chapter 1, the 8086 is a 16-bit microprocessor with a 16-bit data bus and the 8088 is a 16-bit microprocessor with an 8-bit data bus. (As the pin-outs show, the 8086 has pin connections AD0–AD15, and the 8088 has pin connections AD0–AD7.) Data bus width therefore the only major difference between these microprocessors. This allows the 8086 to transfer 16-bit data more efficiently.

There is, however, a minor difference in one of the control signals. The 8088 has an $IO/\overline{M}$ pin, and the 8088 has an $M/\overline{IO}$ pin. The only other hardware difference appears on Pin 34 of both integrated circuits: on the 8088, it is an SS_0 pin, whereas on the 8086, it is a $\overline{BHE}/S7$ pin.

PIN-OUTS AND THE PIN FUNCTIONS:

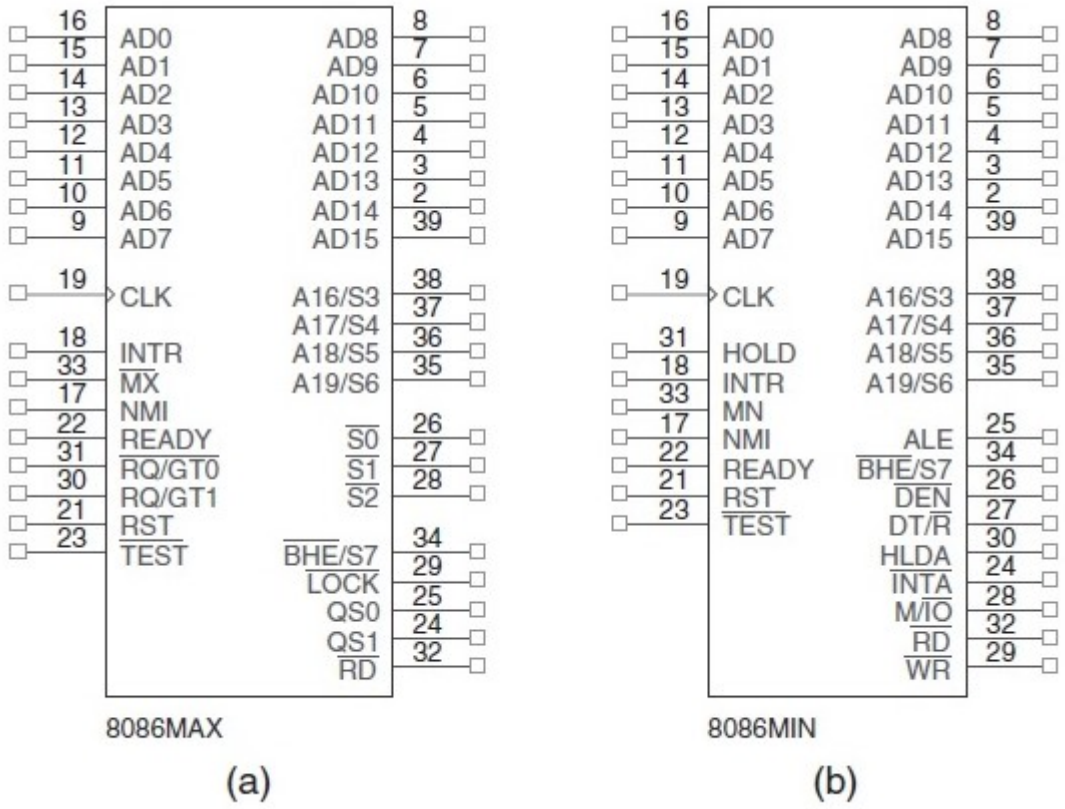

FIGURE 9–1 (a) The pin-out of the 8086 in maximum mode; (b) the pin-out of the 8086 in minimum mode.

AD_7–AD_0 The 8088 address/data bus lines are the multiplexed address data bus of the 8088 and contain the rightmost 8 bits of the memory address or I/O port number whenever ALE is active (logic 1) or data whenever ALE is inactive (logic 0). These pins are at their high-impedance state during a hold Acknowledge.

A15–A8 The 8088 address bus provides the upper-half memory address bits that are present throughout a bus cycle. These address connections go to their high impedance state during a hold acknowledge.

AD15–AD8 The 8086 address/data bus lines compose the upper multiplexed address / data bus on the 8086. These lines contain address bits A15–A8 whenever ALE is a logic 1, and data bus connections D15–D8 when ALE is logic 0. These pins enter a high-impedance state when hold acknowledge occurs.

A19/S6–A16/S3 The address/status bus bits are multiplexed to provide address signals

A19–A16 and also status bits S6–S3. These pins also attain a high-impedance state during the hold acknowledge.

Status bit S6 is always a logic 0, bit S5 indicates the condition of the IF flag bit, and S4 and S3 show which segment is accessed during the current bus cycle. See Table 9–4 for the truth table of S4 and S3. These two status bits could be used to address four separate 1M byte memory banks by decoding them as A21 and A20.

$\overline{RD}$ Whenever the read signal is logic 0, the data bus is receptive to data from the memory or I/O devices connected to the system. This pin floats to its high-impedance state during a hold acknowledge.

READY The READY input is controlled to insert wait states into the timing of the microprocessor. If the READY pin is placed at logic 0 level, the microprocessor enters into wait states and remains idle. If the READY pin is placed at a logic 1 level, it has no effect on the operation of the microprocessor.

INTR INTERRUPT REQUEST is used to request a hardware interrupt. If INTR is held high when IF = 1, the 8086/8088 enters an interrupt acknowledge cycle ($\overline{INTA}$ becomes active) after the current instruction has completed execution.

$\overline{TEST}$ The Test pin is an input that is tested by the WAIT instruction. If $\overline{TEST}$ is a logic 0 is, the WAIT instruction functions as an NOP and if $\overline{TEST}$ is a logic 1, the WAIT instruction is waits for to become a logic 0. The pin is most often connected to the 8087 numeric coprocessor.

NMI The non-maskable interrupt input is similar to INTR except that the NMI interrupt does not check to see whether the IF flag bit is logic 1. If NMI is activated, this interrupt input uses interrupt vector 2.

RESET The reset input causes the microprocessor to reset itself if this pin is held high for a minimum of four clocking periods. Whenever the 8086 or 8088 is reset, it begins executing instructions at memory location FFFFOH and disables future interrupts by clearing the IF flag bit.

CLK The clock pin provides the basic timing signal to the microprocessor. The clock signal must have a duty cycle of 33 % (high for one third of the clocking period and low for two thirds) to provide proper internal timing for the 8086/8088.

VCC This POWER SUPPLY input provides a +5.0 V, ±10 % signal to the microprocessor.

GND The GROUND connection is the return for the power supply. Note that the 8086/8088 microprocessors have two pins labeled GND—both must be connected to ground for proper operation.

$MN/\overline{MX}$ The minimum/maximum mode pin selects either minimum mode or maximum mode operation for the microprocessor. If minimum mode is selected, the $MN/\overline{MX}$ pin must be connected directly to +5.0 V.

$\overline{BHE}/S7$ The bus high enable pin is used in the 8086 to enable the most-significant data bus bits (D15–D8) during a read or a write operation. The state of S7 is always a logic 1.

Minimum Mode Pins:

Minimum mode operation of the 8086/8088 is obtained by connecting the MN/ pin directly to +5.0 V. Do not connect this pin to +5.0 V through a pull-up register or it will not function correctly.

IO/ $\overline{M}$ The IO/ $\overline{M}$ (8088) or the M/ $\overline{IO}$ (8086) pin selects memory or I/O. This pin indicates that the microprocessor address bus contains either a memory address or an I/O port address. This pin is at its high-impedance state during a hold acknowledge.

$\overline{WR}$ The write line is a strobe that indicates that the 8086/8088 is outputting data to a memory or I/O device. During the time that the $\overline{WR}$ is logic 0, the data bus contains valid data for memory or I/O. This pin floats to a high impedance during a hold acknowledge.

$\overline{INTA}$ The interrupt acknowledge signal is a response to the INTR input pin. The $\overline{INTA}$ pin is normally used to gate the interrupt vector number onto the data bus in response to an interrupt request.

ALE ADDRESS LATCH ENABLE shows that the 8086/8088 address/data bus contains address information. This address can be a memory address or an I/O port number. Note that the ALE signal does not float during a hold acknowledge.

DT/$\overline{R}$ The data transmit/receive signal shows that the microprocessor data bus is transmitting (DT/$\overline{R}$) or receiving (DT/$\overline{R}$) data. This signal is used to enable external data bus buffers.

$\overline{DEN}$ Data bus enable activates external data bus buffers.

HOLD The hold input requests a direct memory access (DMA). If the HOLD signal is logic 1, the microprocessor stops executing software and places its address, data, and control bus at the high-impedance state. If the HOLD pin is a logic 0, the microprocessor executes software normally.

HLDA HOLD ACKNOWLEDGE indicates that the 8086/8088 has entered the hold state.

$\overline{SS0}$ The $\overline{SS0}$ status line is equivalent to the S0 pin in maximum mode operation of the microprocessor. This signal is combined with IO/ $\overline{M}$ and DT/$\overline{R}$ to decode the function of the current bus cycle (see Table 9–5).

Maximum Mode Pins:

In order to achieve maximum mode for use with external coprocessors, connect the MN/$\overline{MAX}$ pin to ground.

$\overline{S2}$, $\overline{S1}$ and $\overline{S0}$ The status bits indicate the function of the current bus cycle. These signals are normally decoded by the 8288 bus controller described later in this chapter.

Table 9–6 shows the function of these three status bits in the maximum mode.

$\overline{RQ}$/ $\overline{GT1}$ and $\overline{RQ}$/ $\overline{GT0}$ The REQUEST/GRANT pins request direct memory accesses (DMA) during maximum mode operation. These lines are bidirectional and are used to both request and grant a DMA operation.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	Passive

TABLE 9–5 Bus cycle status (8088) using $\overline{SS0}$.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

TABLE 9–6 Bus control function generated by the bus controller (8288).

QS_1	QS_0	Function
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

TABLE 9–7 Queue status bits.

$\overline{LOCK}$ **The LOCK output is used to lock peripherals off the system. This pin is activated by using the LOCK: prefix on any instruction.**

QS_1 and QS_0 **The queue status bits show the status of the internal instruction queue. These pins are provided for access by the numeric coprocessor (8087). See Table 9–7 for the operation of the queue status bits.**

The 8284A Clock Generator:

The 8284A provides the following basic functions or signals: clock generation, RESET synchronization, READY synchronization, and a TTL-level peripheral clock signal. Figure 9–2 illustrates the pin-out of the 8284A clock generator.

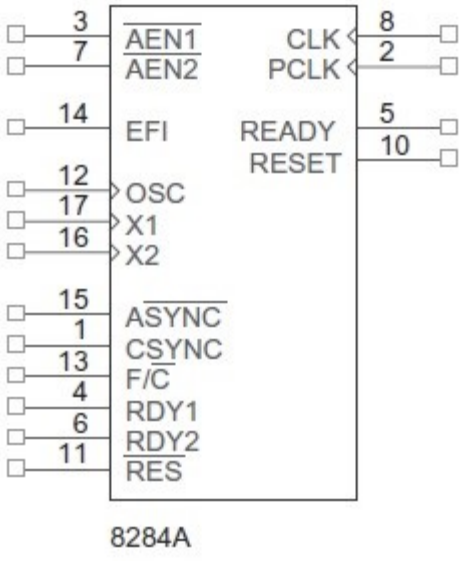

FIGURE 9–2 The pin-out of the 8284A clock generator.

$\overline{AEN1}$ and $\overline{AEN2}$ The address enable pins are provided to qualify the bus ready signals, RDY1 and RDY2, respectively. Section 9–5 illustrates the use of these two pins, which are used to cause wait states, along with the RDY1 and RDY2 inputs. Wait states are generated by the READY pin of the 8086/8088 microprocessors, which is controlled by these two inputs

$\overline{RDY1}$ and $\overline{RDY2}$ The bus ready inputs are provided, in conjunction with the $\overline{AEN1}$ and $\overline{AEN2}$ pins, to cause wait states in an 8086/8088-based system.

$\overline{ASYNC}$ The READY YNCHRONIZATION selection input selects either one or two stages of synchronization for the RDY_1 and RDY_2 inputs.

READY READY is an output pin that connects to the 8086/8088 READY input. This signal is synchronized with the RDY1 and RDY2 inputs.

X_1 and X_2 The CRYSTAL OSCILLATOR pins connect to an external crystal used as the timing source for the clock generator and all its functions.

$F/\overline{C}$ The FREQUENCY/CRYSTAL select input chooses the clocking source for the 8284A. If this pin is held high, an external clock is provided to the EFI input pin; if it is held low, the internal crystal oscillator provides the timing signal. The external frequency input is used when the $F/\overline{C}$ pin is pulled high. EFI supplies the timing whenever the $F/\overline{C}$pin is high.

CLK The CLOCK OUTPUT pin provides the CLK input signal to the 8086/8088 microprocessors and other components in the system. The CLK pin has an output signal that is one third of the crystal or EFI input frequency, and has a 33% duty cycle, which is required by the 8086/8088.

PCLK The **PERIPHERAL CLOCK** signal is one sixth the crystal or EFI input frequency, and has a 50% duty cycle. The PCLK output provides a clock signal to the peripheral equipment in the system.

OSC The **OSCILLATOR OUTPUT** is a TTL-level signal that is at the same frequency as the crystal or EFI input. The OSC output provides an EFI input to other 8284A clock generators in some multiple-processor systems.

$\overline{\text{RES}}$ The reset input is an active-low input to the 8284A. The $\overline{\text{RES}}$ pin is often connected to an RC network that provides power-on resetting.

RESET The reset output is connected to the 8086/8088 RESET input pin.

CSYNC The clock synchronization pin is used whenever the EFI input provides synchronization in systems with multiple processors. If the internal crystal oscillator is used, this pin must be grounded.

GND The ground pin connects to ground.

VCC This power supply pin connects to +5.0 V with a tolerance of ±10%.

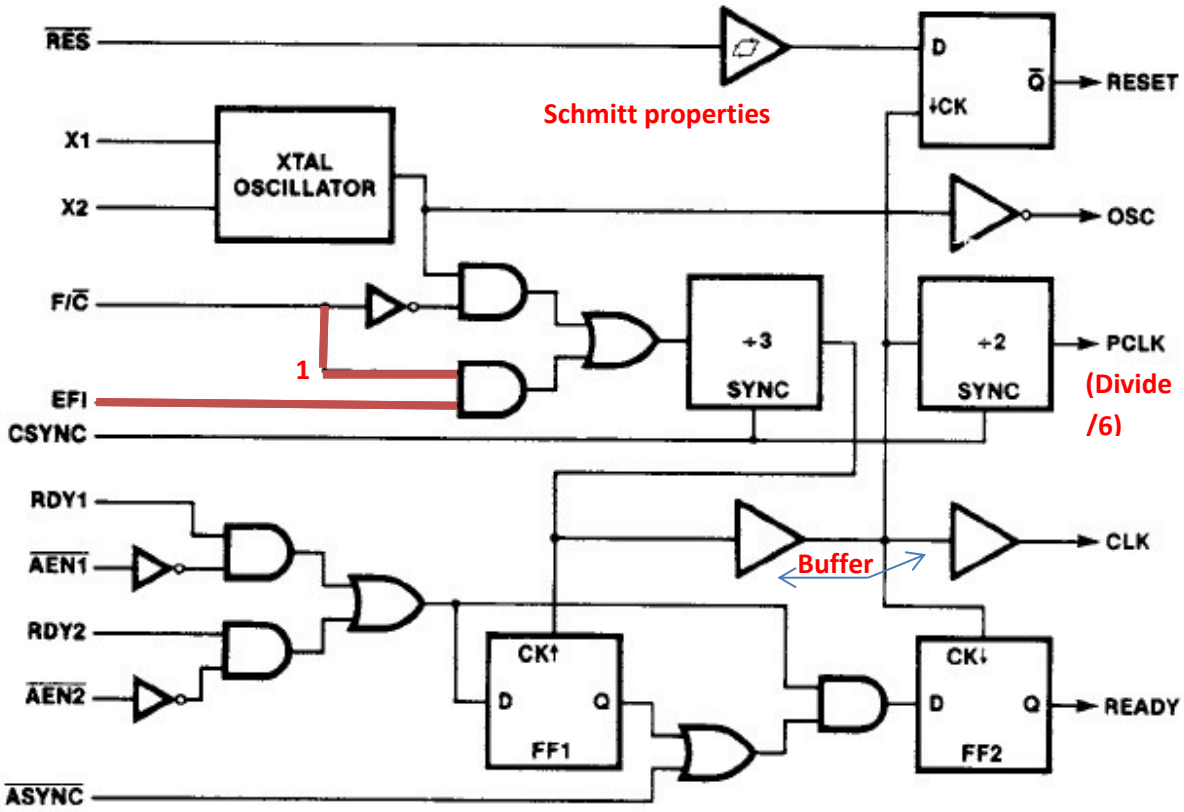

FIGURE 9–3 The internal block diagram of the 8284A clock generator.

- If a crystal is attached to X1 and X2, the oscillator generates a square wave signal at the same frequency as the crystal.
- When $\text{F}/\overline{\text{C}}$ is logic 0, the oscillator output is steered through to the divide-by-3 counter. If $\text{F}/\overline{\text{C}}$ is a logic 1, then EFI is steered through to the counter.

- **The output of the divide-by-3 counter generates the timing for ready synchronization, a signal for another counter (divide-by-2), and the CLK signal to the 8086/8088 microprocessor.**
- **Provide the divide-by-6 output at PCLK, the peripheral clock output.**

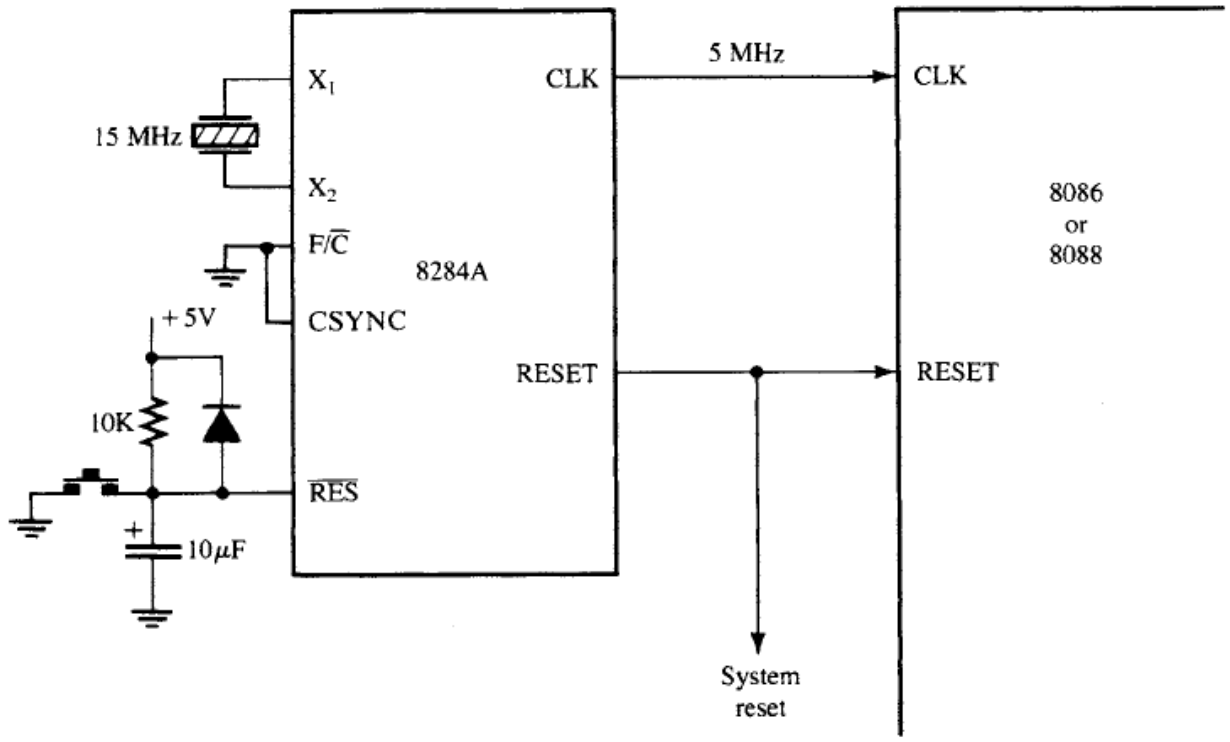

FIGURE 9–4 The clock generator (8284A) and the 8086 and 8088 microprocessors illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor.

<u>Operation of the Reset Section:</u> It consists of a Schmitt trigger buffer and a single D-type flip-flop circuit. The D-type flip-flop ensures that the timing requirements of the 8086/8088 RESET input are met. This circuit applies the RESET signal to the microprocessor on the negative edge (1-to-0 transition) of each clock.
The flip-flop makes certain that RESET goes high in four clocks, and the RC time constant ensures that it stays high for at least 50 μs.