## BUS TIMING:

**The 8086/8088 microprocessors use the memory and I/O in periods called bus cycles. Each bus cycle equals four system-clocking periods (T states). Newer microprocessors divide the bus cycle into as few as two clocking periods. If the clock is operated at 5 MHz (the basic operating frequency for these two microprocessors), one 8086/8088 bus cycle is complete in 800 ns.**

**If data are written to the memory (see the simplified timing for write in Figure 9–9), the microprocessor outputs the memory address on the address bus, outputs the data to be written into memory on the data bus, and issues a write ($\overline{WR}$ ) to memory and $IO/\overline{M}$ = 0 for the 8088 and $M/\overline{IO}$ = 1 for the 8086. If data are read from the memory (see the simplified timing for read in Figure 9–10), the microprocessor outputs the memory address on the address bus, issues a read memory signal ($\overline{RD}$), and accepts the data via the data bus.**

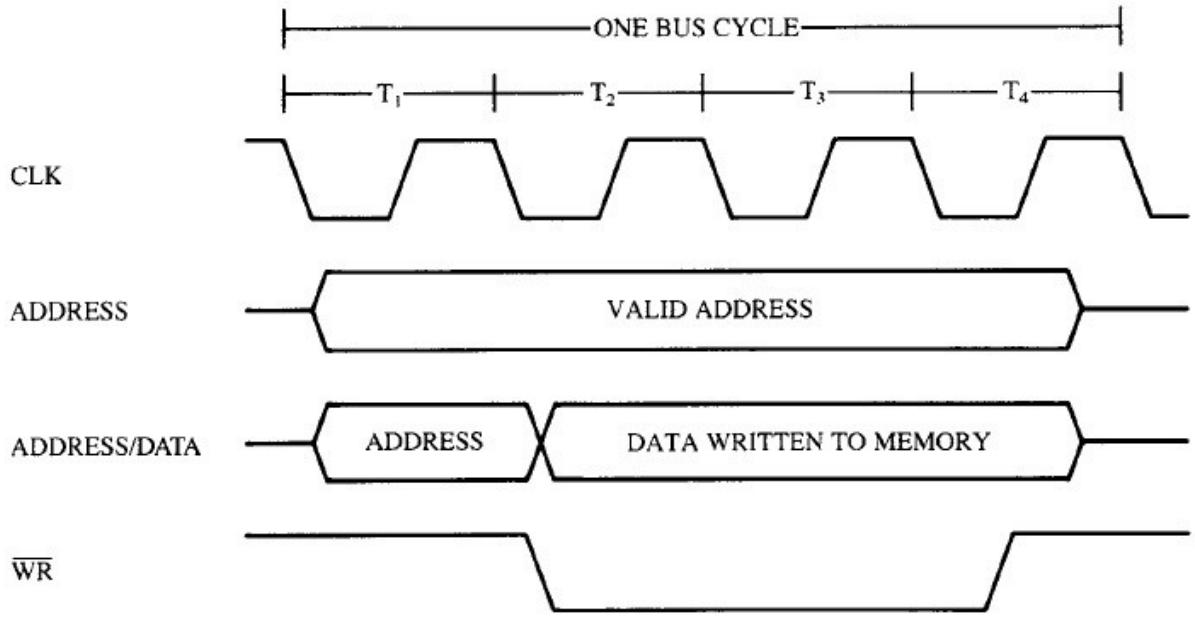



**FIGURE 9–9 Simplified 8086/8088 write bus cycle.**

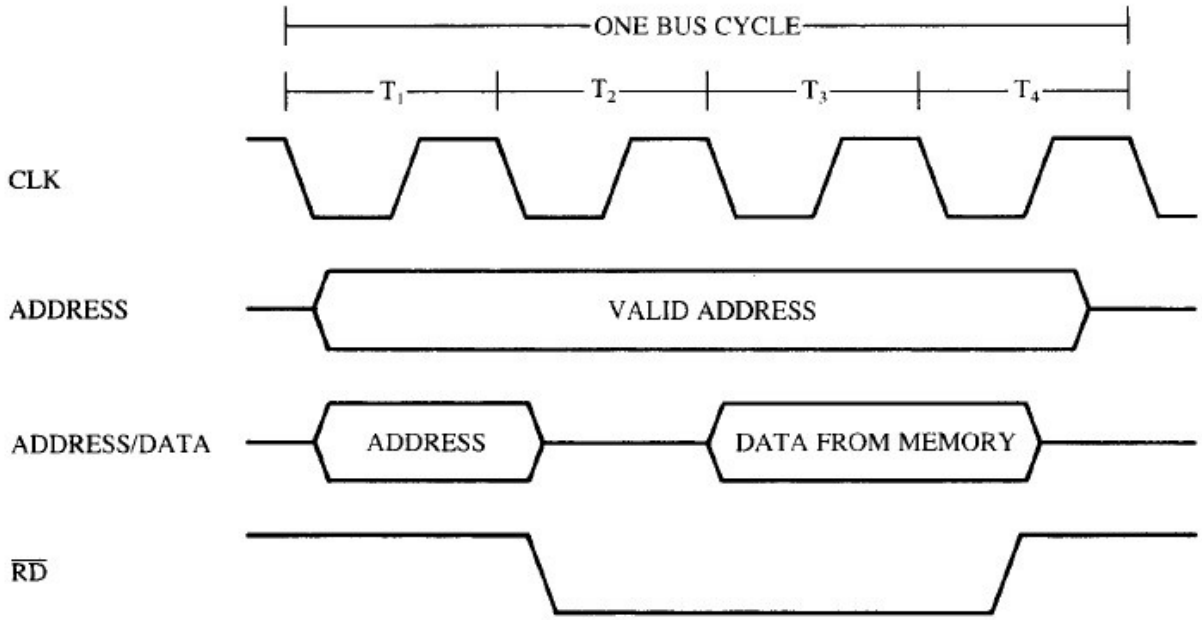



**FIGURE 9–10 Simplified 8086/8088 read bus cycle.**

- **At the first clocking period in a bus cycle T1:**

**The address of the memory or I/O location is sent out via the address bus and the address/data bus connections. (The address/data bus is multiplexed and sometimes contains memory-addressing information, sometimes data.) During TI, control signals ALE, $DT/\overline{R}$ , and $IO/\overline{M}$ (8088) or $M/\overline{IO}$ (8086) are also output. The $IO/\overline{M}$ or $M/\overline{IO}$ signal indicates whether the address bus contains a memory address or an I/O device (port) number.**

- **During T2:**

**The $\overline{RD}$ or $\overline{WR}$ signal, DEN, and in the case of a write, the data to be written appear on the data bus. These events cause the memory or I/O device to begin to perform a read or a write. The $\overline{DEN}$ signal TURNS ON the data bus buffers, If this happens to be a write bus cycle, the data are sent out to the memory or I/O through the data bus. READY is sampled at the end of $T_2$ , If READY is low at this time, T3 becomes a wait state (Tw)**

- **During Tw:**

**This clocking period is provided to allow the memory time to access data. If the bus cycle happens to be a read bus cycle, the data bus is sampled at the end of T3.**

- **During T4:**

**All bus signals are deactivated in preparation for the next bus cycle. This is also the time when the 8086/8088 samples the data bus connections for data that are read from memory or I/O. In addition, at this point, the trailing edge of the $\overline{WR}$ signal transfers data to the memory or I/O, which activates and writes when the $\overline{WR}$ signal returns to logic 1 level.**

## Read Timing:

**The most important item contained in the read timing diagram is the amount of time allowed for the memory or I/O to read the data.**
**You will notice a line that extends from the end of T3 down to the data bus. At the end of T3, the microprocessor samples the data bus.**
**Memory access time starts when the address appears on the memory address bus and continues until the microprocessor samples the memory data at T3. Approximately three T states elapse between these times. The address does not appear until $T_{CLAV}$ time (110 ns if the clock is 5 MHz) after the start of T1.**
**Memory access time is three clocking states minus the sum of $T_{CLAV}$ and $T_{DVCL}$. Because $T_{DVCL}$ is 30 ns with a 5 MHz clock, the allowed memory access time is only 460 ns (access time = 600 ns - 110 ns - 30 ns).**
**NOTE: The memory devices chosen for connection to the 8086/8088 operating at 5 MHz must be able to access data in less than 460 ns.**

**The only other timing factor that may affect memory operation is the width of the $\overline{RD}$ strobe. On the timing diagram, the read strobe is given as $T_{RLRH}$. The time for this strobe is 325 ns (5 MHz clock rate), which is wide enough for almost all memory devices manufactured with an access time of 400 ns or less.**

## Write Timing:

**Figure 9–13 illustrates the write-timing diagram for the 8088 microprocessor. (Again, the 8086 is nearly identical, so it need not be presented here in a separate timing diagram.) The main differences between read and write timing are minimal. The $\overline{RD}$ strobe is replaced by the $\overline{WR}$ strobe; the data bus contains information for the memory rather than information from the memory, and $DT/\overline{R}$ remains a logic 1 instead of a logic 0 throughout the bus cycle.**
**Memory data are written at the trailing edge of the $\overline{WR}$ strobe. According to the timing diagram, this critical period is $T_{WHDX}$ or 88 ns when the 8088 is operated with a 5 MHz clock. The width of the $\overline{WR}$ strobe is $T_{WLWH}$ or 340 ns at a 5 MHz clock rate. This rate is compatible with most memory devices that have an access time of 400 ns or less.**

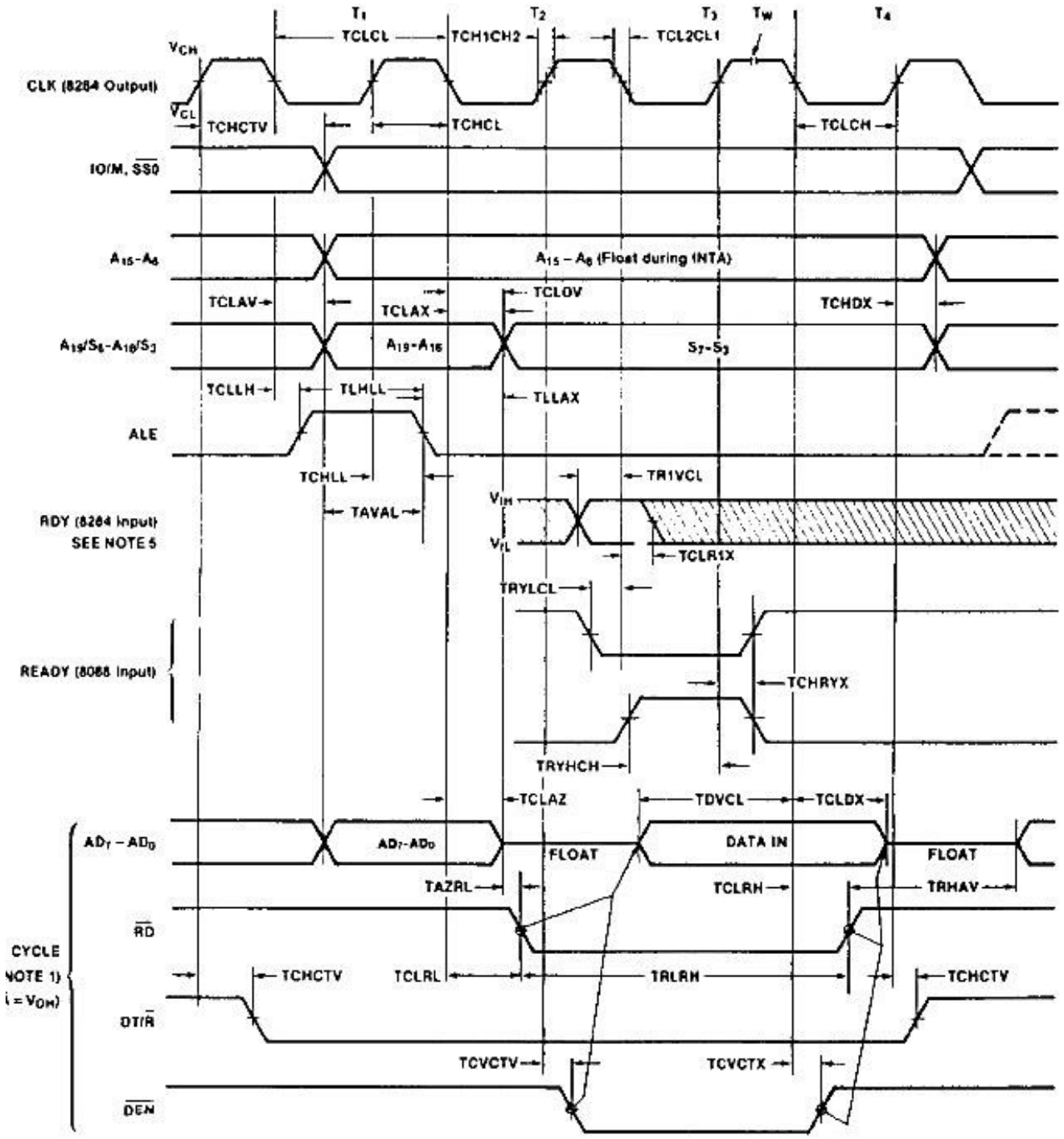
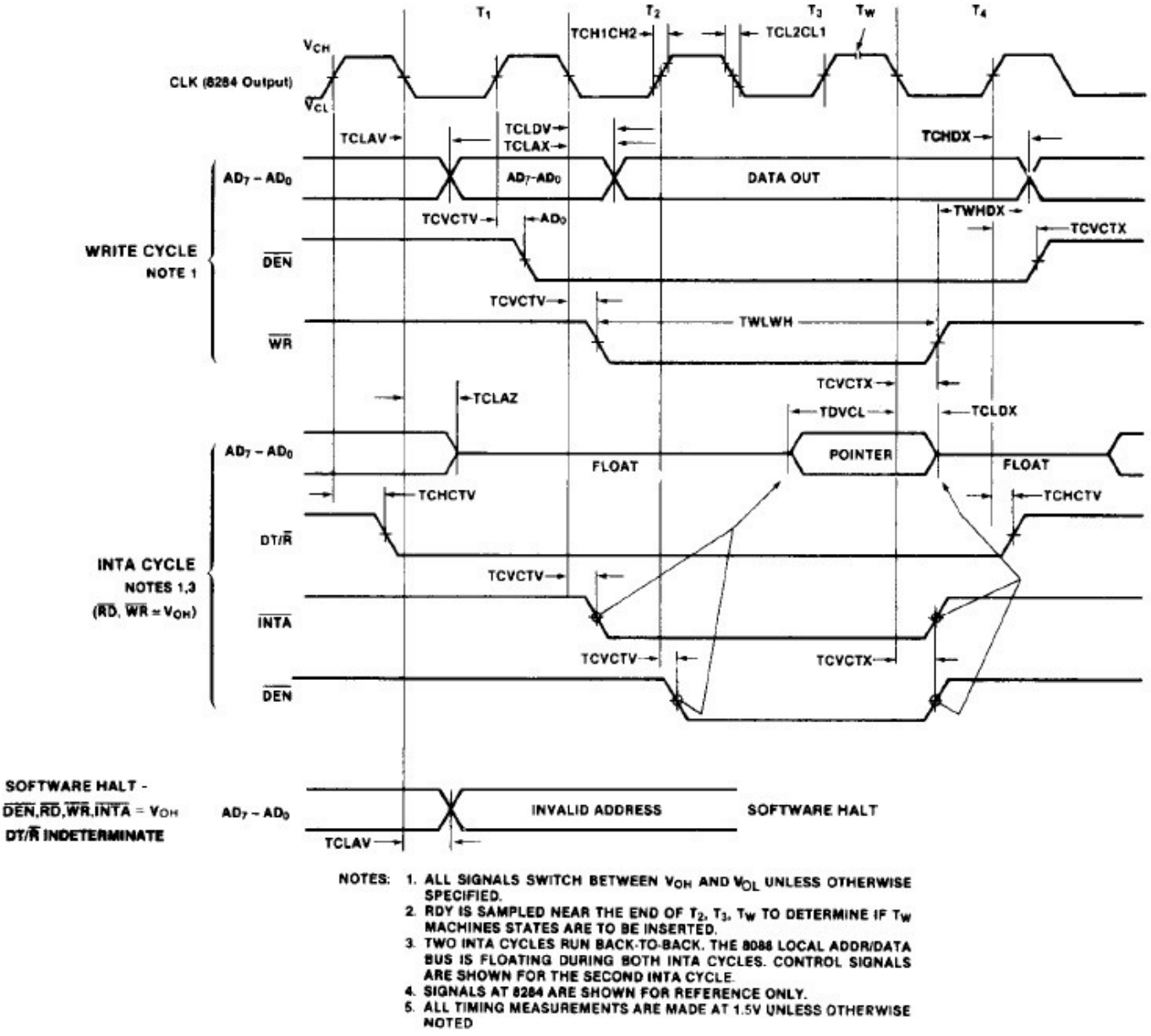



**FIGURE 9–11 Minimum mode 8088 bus timing for a read operation.**




NOTES:
1. ALL SIGNALS SWITCH BETWEEN $V_{OH}$ AND $V_{OL}$ UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF $T_2$, $T_3$, $T_W$ TO DETERMINE IF $T_W$ MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED

**FIGURE 9–13 Minimum mode 8088 write bus timing.**

**READY AND THE WAIT STATE: The READY input causes wait states for slower memory and I/O components. A wait state (Tw) is an extra clocking period, inserted between T2 and T3 to lengthen the bus cycle. If one wait state is inserted, then the memory access time, normally 460 ns with a 5 MHz clock, is lengthened by one clocking period (200 ns) to 660 ns.**

**Figure 9–17 illustrates a circuit used to introduce almost any number of wait states for the 8086/8088 microprocessors. Here, an 8-bit serial shift register (74LS164) shifts a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A. The output of the register is forced high**

**when the $\overline{RD}$, $\overline{WR}$ , and $\overline{INTA}$ pins are all logic 1s. These three signals are high until state $T_2$, so the shift register shifts for the first time when the positive edge of the $T_2$ arrives. If one wait is desired, output QB is connected to the OR gate. If two waits are desired, output QC is connected, and so forth.**

**Figure 9–18 illustrates the timing diagram for this shift register wait state generator when it is wired to insert one wait state.**

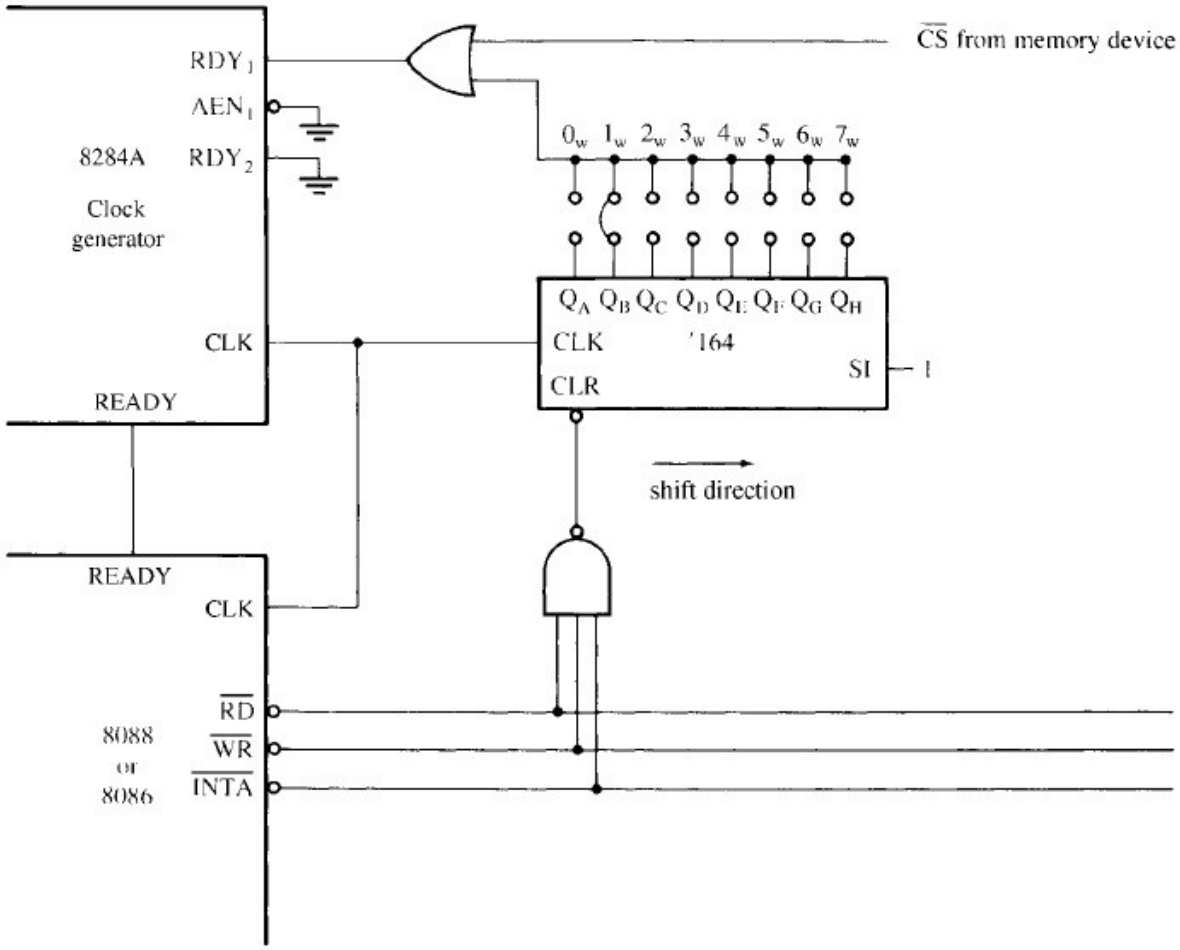



**FIGURE 9–17 A circuit that will cause between 0 and 7 wait states.(One wait state is generated ).**