SUMMARY:

1. The main differences between the 8086 and 8088 are (1) an 8-bit data bus on the 8088 and a 16-bit data bus on the 8086, (2) an $\overline{SS0}$ pin on the 8088 in place of $\overline{BHE}/S7$ on the 8086, and (3) an $IO/\overline{M}$ pin on the 8088 instead of an $M/\overline{IO}$ on the 8086.

2. Both the 8086 and 8088 require a single +5.0 V power supply with a tolerance of ±10%.

3. The 8086/8088 microprocessors are TTL-compatible if the noise immunity figure is de-rated to 350 mV from the customary 400 mV.

4. The 8086/8088 microprocessors can drive one 74XX, five 74LSXX, one 74SXX, ten 74ALSXX, and ten 74HCXX unit loads.

5. The 8284A clock generator provides the system clock (CLK), READY synchronization, and RESET synchronization.

6. The standard 5 MHz 8086/8088 operating frequency is obtained by attaching a 15 MHz crystal to the 8284A clock generator. The PCLK output contains a TTL-compatible signal at one half the CLK frequency.

7. Whenever the 8086/8088 microprocessors are reset, they begin executing software at memory location FFFF0H (FFFF:0000) with the interrupt request pin disabled.

8. Because the 8086/8088 buses are multiplexed and most memory and I/O devices aren't, the system must be demultiplexed before interfacing with memory or I/O. Demultiplexing is accomplished by an 8-bit latch whose clock pulse is obtained from the ALE signal.

9. In a large system, the buses must be buffered because the 8086/8088 microprocessors are capable of driving only 10 unit loads, and large systems often have many more.

10. Bus timing is very important to the remaining chapters in the text. A bus cycle that consists of four clocking periods acts as the basic system timing. Each bus cycle is able to read or write data between the microprocessor and the memory or I/O system.

11. A bus cycle is broken into four states, or T periods: T1 is used by the microprocessor to send the address to the memory or I/O and the ALE signal to the demultiplexers; T2 is used to send data to memory for a write and to test the READY pin and activate control signals $\overline{RD}$ or $\overline{WR}$; T3 allows the memory time to access data and allows data to be transferred between the microprocessor and the memory or I/O; and T4 is where data are written.

12. The 8086/8088 microprocessors allow the memory and I/O 460 ns to access data when they are operated with a 5 MHz clock.

13. Wait states (T_w) stretch the bus cycle by one or more clocking periods to allow the memory and I/O additional access time. Wait states are inserted by controlling the READY input to the 8086/8088. READY is sampled at the end of T_2 and during T_w.

14. Minimum mode operation is similar to that of the Intel 8085A microprocessor, whereas maximum mode operation is new and specifically designed for the operation of the 8087 arithmetic coprocessor.

15. The 8288 bus controller must be used in the maximum mode to provide the control bus signals to the memory and I/O. This is because the maximum mode operation of the 8086/8088 removes some of the system's control signal lines in favor of control signals for the coprocessors. The 8288 reconstructs these removed control signals.

QUESTIONS AND PROBLEMS:

1. List the differences between the 8086 and the 8088 microprocessors.
2. Is the 8086/8088 TTL-compatible? Explain your answer.
3. What is the fan-out from the 8086/8088 to the following devices:
(a) 74XXX TTL
(b) 74ALSXXX TTL
(c) 74HCXXX CMOS
4. What information appears on the address/data bus of the 8088 while ALE is active?
5. What are the purposes of status bits S3 and S4?
6. What condition does logic 0 on the 8086/8088 $\overline{\text{RD}}$ pin indicate?
7. Explain the operation of the $\overline{\text{TEST}}$ pin and the WAIT instruction.
8. Describe the signal that is applied to the CLK input pin of the 8086/8088 microprocessors.
9. What mode of operation is selected when $\text{MN}/\overline{\text{MAX}}$ is grounded?
10. What does the $\overline{\text{WR}}$ strobe signal from the 8086/8088 indicate about the operation of the 8086/8088?
11. When does ALE float to its high-impedance state?
12. When $\text{DT}/\overline{\text{R}}$ is a logic 1, what condition does it indicate about the operation of the 8086/8088?
13. What happens when the HOLD input to the 8086/8088 is placed at its logic 1 level?
14. What three minimum mode 8086/8088 pins are decoded to discover whether the processor is halted?
15. Explain the operation of the $\overline{\text{LOCK}}$ pin.
16. What conditions do the QS1 and QS0 pins indicate about the 8086/8088?
17. What three housekeeping chores are provided by the 8284A clock generator?
18. By what factor does the 8284A clock generator divide the crystal oscillator's output frequency?
19. If the $\text{F}/\overline{\text{C}}$ pin is placed at logic 1 level, the crystal oscillator is disabled. Where is the timing input signal attached to the 8284A under this condition?
20. The PCLK output of the 8284A is _____ MHz if the crystal oscillator is operating at 14 MHz.
21. The $\overline{\text{RES}}$ input to the 8284A is placed at a logic _____ level in order to reset the 8086/8088.
22. Which bus connections on the 8086 microprocessor are typically demultiplexed?
23. Which bus connections on the 8088 microprocessor are typically demultiplexed?

24. Which TTL-integrated circuit is often used to demultiplex the buses on the 8086/8088?
25. What is the purpose of the demultiplexed $\overline{\text{BLE}}$ signal on the 8086 microprocessor?
26. Why are buffers often required in an 8086/8088-based system?
27. What 8086/8088 signal is used to select the direction of the data flows through the 74LS245 bidirectional bus buffer?
28. A bus cycle is equal to clocking _____ periods.
29. If the CLK input to the 8086/8088 is 4 MHz, how long is one bus cycle?
30. What two 8086/8088 operations occur during a bus cycle?
31. How many MIPS is the 8086/8088 capable of obtaining when operated with a 10 MHz clock?
32. Briefly describe the purpose of each T state listed:
(a) T1 (b) T2 (c) T3 (d) T4 (e) Tw
33. How much time is allowed for memory access when the 8086/8088 is operated with a 5 MHz clock?
34. How wide is $\overline{\text{DEN}}$ if the 8088 is operated with a 5 MHz clock?
35. If the READY pin is grounded, it will introduce_____ states into the bus cycle of the 8086/8088.
36. What does the $\overline{\text{ASYNC}}$ input to the 8284A accomplish?
37. What logic levels must be applied to $\overline{\text{AEN1}}$ and RDY1 to obtain a logic 1 at the READY pin? (Assume that $\overline{\text{AEN2}}$ is at logic 1 level.)
38. Contrast minimum and maximum mode 8086/8088 operation.
39. What main function is provided by the 8288 bus controller when used with 8086/8088 maximum mode operation?