Chapter 10

Memory Interface

MEMORY DEVICES

Memory Pin Connections

Pin connections common to all memory devices are the address inputs, data outputs or input/outputs, some type of selection input, and at least one control input used to select a read or write operation. See Figure 10–1 for ROM and RAM generic-memory devices.

Address Connections. All memory devices have address inputs that select a memory location within the memory device. Address inputs are almost always labeled from A_0, the least significant address input, to a_n where subscript n can be any value but is always labeled as one less than the total number of address pins. For example, a memory device with 10 address pins has its address pins labeled from A_0 to A_9. The number of address pins found on a memory device is determined by the number of memory locations found within it.

A 1K memory device has 10 address pins (A_0–A_9); therefore, 10 address inputs are required to select any of its 1024 memory locations. It takes a 10-bit binary number (1024 different combinations) to select any single location on a 1024-location device. If a memory device has 11 address connections (A_0–A_{11}), it has 2048 (2K) internal memory locations. The number of memory locations can thus be extrapolated from the number of address pins. For example, a 4K memory device has 12 address connections, an 8K device has 13, and so forth. A device that contains 1M locations requires a 20-bit address (A_0–A_{19}).

Data Connections: All memory devices have a set of data outputs or input/outputs. The device illustrated in Figure 10–1 has a common set of input/output (I/O) connections. Many memory devices have bidirectional common I/O pins.

An 8-bit-wide memory device is often called a byte-wide memory. Although most devices are currently 8 bits wide, some devices are 16 bits, 4 bits, or just 1 bit wide.

Selection Connections: Each memory device has an input—sometimes more than one—that selects or enables the memory device. This type of input is most often called a chip select ($\overline{CS}$), chip enable ($\overline{CE}$), or simply select ($\overline{S}$) input. RAM memory generally has at least one $\overline{CS}$ or $\overline{S}$ input, and ROM has at least one $\overline{CE}$. If the $\overline{CS}$, $\overline{CE}$ or $\overline{S}$ input is active (a logic 0, in this case, because of the over bar), the memory device performs a read or write operation; if it is inactive (a logic 1, in this case), the memory device cannot do a read or a write because it is turned off or disabled. If more than one $\overline{CS}$ connection is present, all must be activated to read or write data.

Control Connections. All memory devices have some form of control input or inputs. A ROM usually has only one control input, while a RAM often has one or two control inputs.

The control input most often found on a ROM is the output enable ($\overline{OE}$) or gate ($\overline{G}$) connection, which allows data to flow out of the output data pins of the ROM. If $\overline{OE}$ and the selection input ($\overline{CE}$) are both active, the output is enabled; if $\overline{OE}$ is inactive, the output is disabled at its high-impedance state. The $\overline{OE}$ connection enables and disables a set of three-state buffers located within the memory device and must be active to read data.

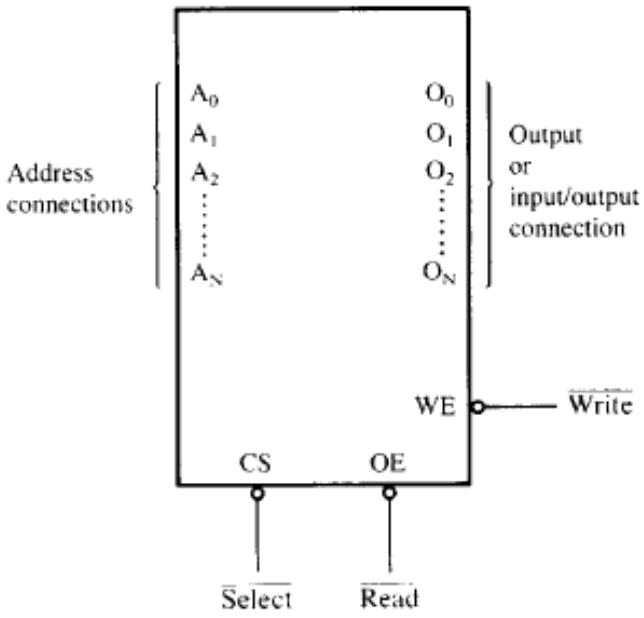


FIGURE 10–1 A pseudo memory component illustrating the address, data, and control connections.

A RAM memory device has either one or two control inputs. If there is only one control input, it is often called $R/\overline{W}$. This pin selects a read operation or a write operation only if the device is selected by the selection input ($\overline{CE}$). If the RAM has two control inputs, they are usually labeled ($\overline{WE}$or $\overline{W}$), and $\overline{OE}$ (or $\overline{G}$). Here, $\overline{WE}$ (write enable) must be active to perform a memory write, and $\overline{OE}$ must be active to perform a memory read operation. When these two controls ($\overline{WE}$ and $\overline{OE}$) are present, they must never both be active at the same time. If both control inputs are inactive (logic 1s), data are neither written nor read, and the data connections are at their high-impedance state.

ROM Memory

The read-only memory (ROM) permanently stores programs and data that are resident to the system and must not change when power supply is disconnected. The ROM is permanently programmed so that data are always present, even when power is disconnected. This type of memory is often called nonvolatile memory, because its contents *do not* change even if power is disconnected.

The ROM is available in many forms. The EPROM (erasable programmable read-only memory), a type of ROM, is more commonly used when software must be changed often or when too few are in demand to make the ROM economical. An EPROM is programmed in the field on a device called an EPROM programmer. The EPROM is also erasable if exposed to high-intensity ultraviolet light for about 20 minutes or so, depending on the type of EPROM.

The PROM (programmable read-only memory) is also programmed in the field by burning open tiny NI-chrome or silicon oxide fuses; but once it is programmed, it cannot be erased.

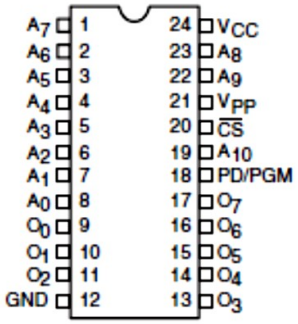
Newer type of read-mostly memory (RMM) is called the flash memory. The flash memory[1] is also often called an EEPROM (electrically erasable programmable ROM), EAROM (electrically alterable ROM), or a NOVRAM (nonvolatile RAM). These memory devices are electrically erasable in the system, but they require more time to erase than a normal RAM.

The flash memory device is used to store setup information for systems such as the video card in the computer. It has all but replaced the EPROM in most computer systems for the BIOS memory. Some systems contain a password stored in the flash memory device. Flash Memory has its biggest impact in memory cards for digital cameras and memory in MP3 audio players.
Figure 10–2 illustrates the 2716 EPROM, which is representative of most common EPROMs. This device contains 11 address inputs and eight data outputs. The 2716 is a 2K · 8 read-only memory device. The 27XXX series of the EPROMs includes the following part numbers:
2704 (512 · 8), 2708 (1K · 8), 2716 (2K · 8), 2732 (4K · 8), 2764 (8K · 8), 27128 (16K · 8), 27256 (32K · 8), 27512 (64K · 8), and 271024 (128K · 8). Each of these parts contains address pins, eight data connections, one or more chip selection inputs ($\overline{CE}$), and an output enable pin ($\overline{OE}$).

MODE SELECTION

PINS / MODE	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

BLOCK DIAGRAM

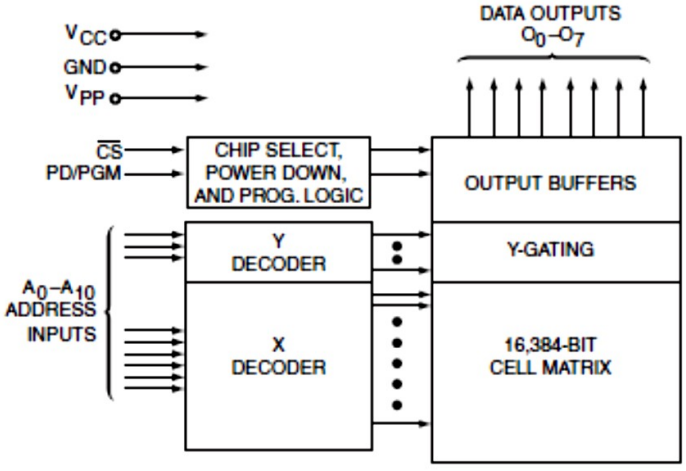


FIGURE 10–2 The pin-out of the 2716, 2K · 8 EPROM. (Courtesy of Intel Corporation.)

Figure 10–3 illustrates the timing diagram for the 2716 EPROM. Data appear on the output connections only after logic 0 is placed on both $\overline{CE}$ and $\overline{OE}$ pin connections. If $\overline{CE}$ and $\overline{OE}$ are not both logic 0s, the data output connections remain at their high-impedance or off states.

Note that the V_{PP} pin must be placed at logic 1 level for data to be read from the EPROM. In some cases, the V_{PP} pin is in the same position as the $\overline{WE}$ pin on the SRAM. This will allow a single socket to hold either an EPROM or an SRAM. An example is the 27256 EPROM and the

62256 SRAM, both 32K · 8 devices that have the same pin-out, except for V_{PP} on the EPROM and $\overline{WE}$ on the SRAM.

A.C. Characteristics

T_A = 0°C to 70°C, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

Capacitance[5] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

WAVEFORMS

A. Read Mode

PD/PGM = V_{IL}

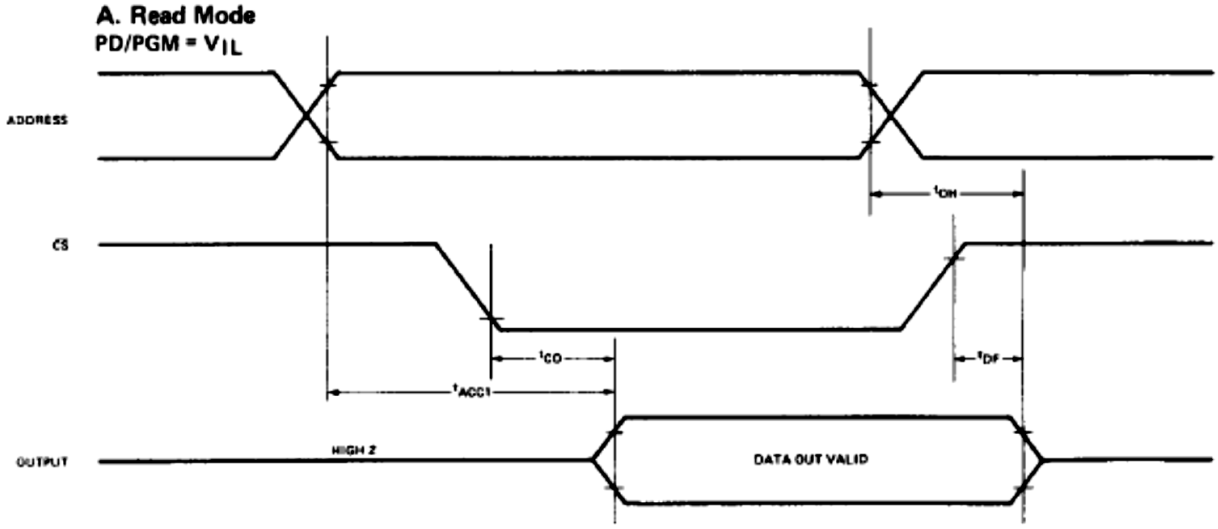


FIGURE 10–3 The timing diagram of AC characteristics of the 2716 EPROM. (Courtesy of Intel Corporation.)

One important piece of information provided by the timing diagram and data sheet is the memory access time—the time that it takes the memory to read information. As Figure 10–3 illustrates, memory access time (T_{ACC}) is measured from the appearance of the address at the address inputs until the appearance of the data at the output connections. This is based on the assumption that the $\overline{CE}$ input goes low at the same time that the address inputs become stable. Also, $\overline{OE}$ must be logic 0 for the output connections to become active. The basic speed of this EPROM is 450 ns. (Recall that the 8086/8088 operated with a 5 MHz clock allowed memory 460 ns to access data.) This type of memory component requires wait states to operate properly with the 8086/8088 microprocessors because of its rather long access time. If the wait states are not desired, higher-speed versions of the EPROM are available at an additional cost. Today, EPROM memory is available with access times of as little as 100 ns. Obviously, wait states are required in modern microprocessors for any EPROM device.

Static RAM (SRAM) Devices:

Static RAM memory devices retain data for as long as DC power is applied. Because no special action (except power) is required to retain stored data, these devices are called static memory.

They are also called volatile memory because they will not retain data without power. The main

Figure 10–5 depicts the timing diagram for the 4016 SRAM. As the read cycle timing reveals, the access time is $t_{a(A)}$. On the slowest version of the 4016, this time is 250 ns, which is fast enough to connect directly to an 8088 or an 8086 operated at 5 MHz without wait states.

Again, it is important to remember that the access time must be checked to determine the compatibility of memory components with the microprocessor.

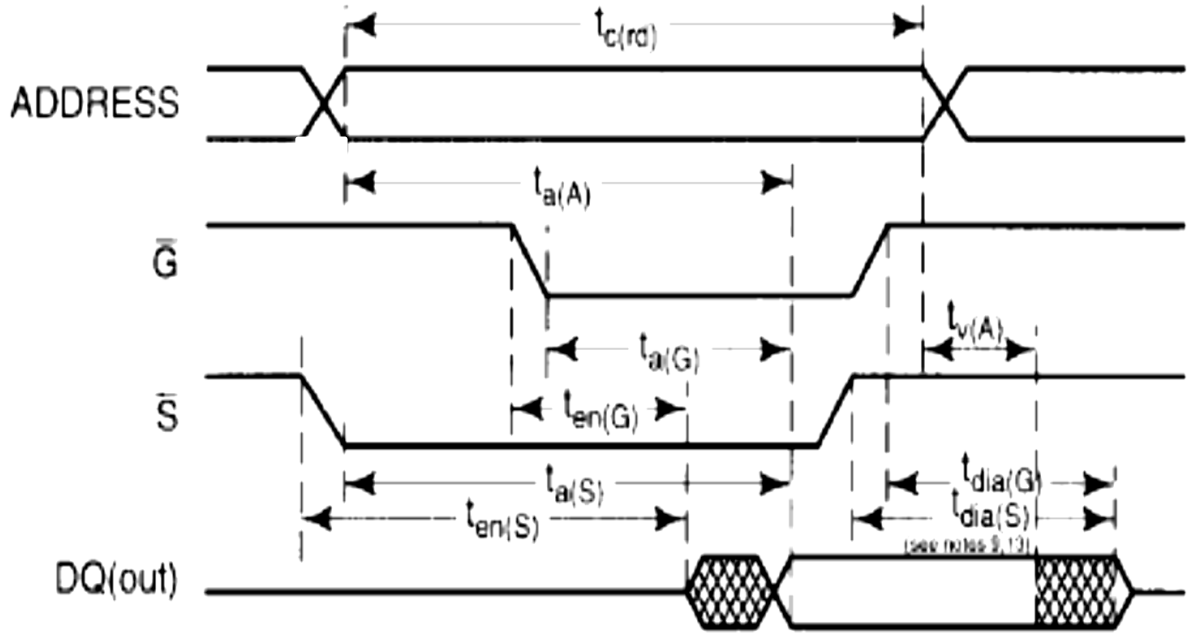
Figure 10–6 illustrates the pin-out of the 62256, 32K · 8 static RAM. This device is packaged in a 28-pin integrated circuit and is available with access times of 120 ns or 150 ns.

TMS4016 . . . NL PACKAGE
(TOP VIEW)

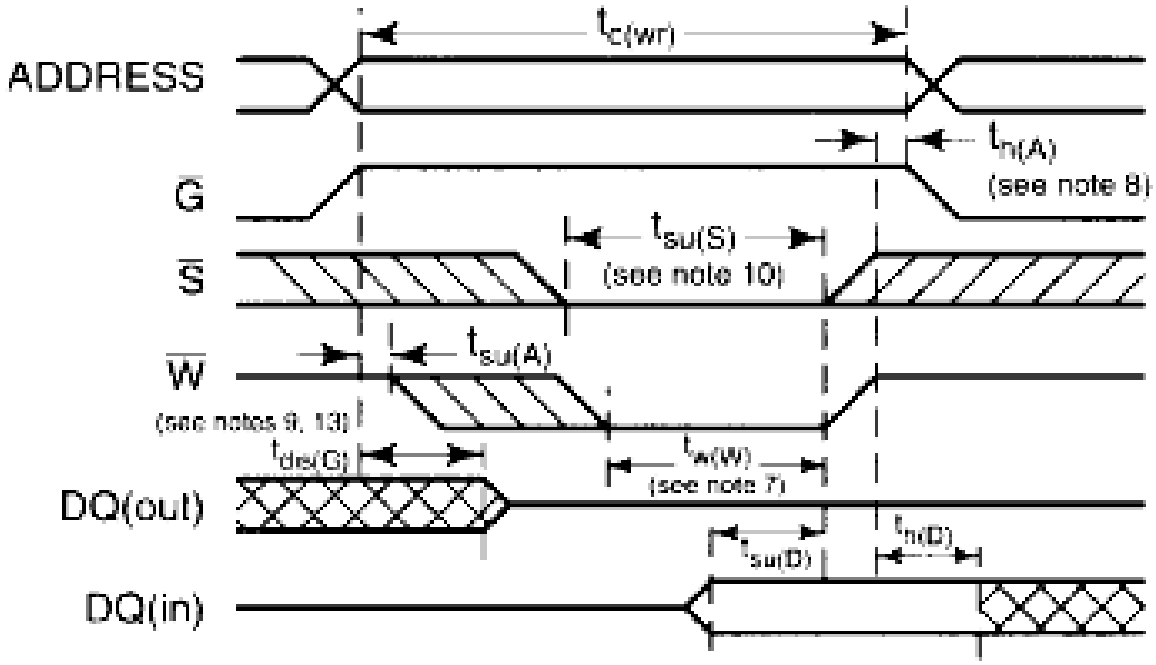
PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

FIGURE 10–4 The pin-out of the TMS4016, 2K · 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)

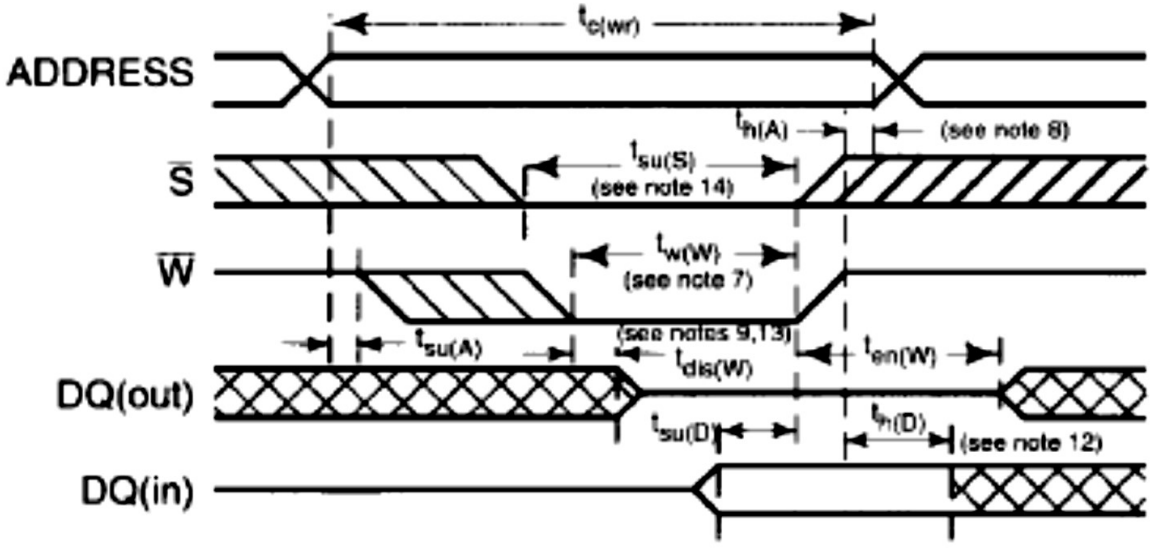
Other common SRAM devices are available in 8K · 8, 128K · 8, 256K · 8, 512K · 8, and 1M · 8 sizes, with access times of as little as 1.0 ns for SRAM used in computer cache memory systems.



Timing waveform of read cycle (note 5)



Timing waveform of write cycle no.1 (note 6)



Timing waveform of write cycle no.2 (see notes 6 & 11)

NOTES:

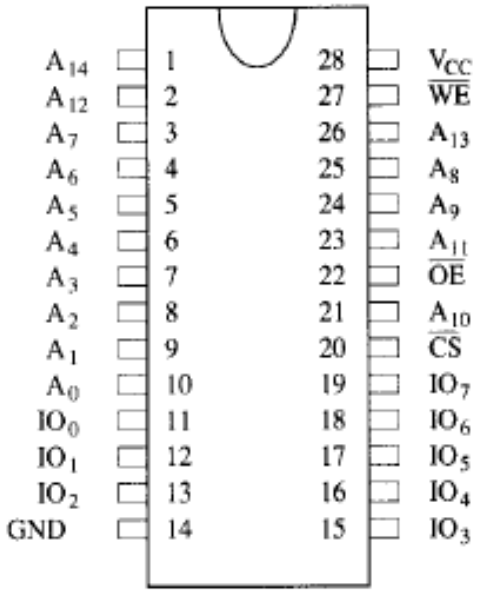
5. **W is high Read Cycle.**
6. **W must be high during all address transitions.**
7. **A write occurs during the overlap of a low S and a low W.**
8. **Th(A)is measured from the earlier of S or W going high to the end of the write cycle.**
9. **During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.**
10. **If the Slow transition occurs simultaneously with the W low transitions or alter the W transition, outputs remains in a high impedance state.**
11. **G is continuously low ($G = V_{IL}$).**
12. **If S is low during this period, I/O pins are in the output state. Data input signals of opposite phase to outputs must not be applied.**
13. **Transition is measured ±200 mV from steady-state voltage.**
14. **If the S low transition occurs before the W low transition, then the data input signals of opposite phase to the outputs must not be applied.**

FIGURE 10–5 The timing diagrams of the TMS4016 SRAM. (Courtesy of Texas Instruments Incorporated.)

Another disadvantage of DRAM memory is that it requires so many address pins that the manufacturers have decided to multiplex the address inputs. Figure 10–7 illustrates a 64K · 4 DRAM, the TMS4464, which stores 256K bits of data. Notice that it contains only eight address inputs where it should contain 16—the number required to address 64K memory locations. The only way that 16 address bits can be forced into eight address pins is in two 8-bit increments.

This operation requires two special pins: the column address strobe ($\overline{CAS}$) and row address strobe ($\overline{RAS}$).

First, A_0–A_7 are placed on the address pins and strobed into an internal row latch by $\overline{RAS}$ as the row address. Next, the address bits A_8-A_{15} are placed on the same eight address inputs and strobed into an internal column latch by as the column address (see Figure 10–8 for this timing). The 16-bit address held in these internal latches addresses the contents of one of the 4-bit memory locations. Note that also performs the function of the chip selection input to the DRAM.



PIN FUNCTION

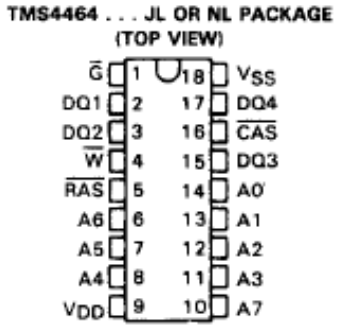
A_0 - A_{14}	Addresses
IO_0 - IO_7	Data connections
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V Supply
GND	Ground

FIGURE 10–6 Pin diagram of the 62256, 32K · 8 static RAM.

Figure 10–9 illustrates a set of multiplexers used to strobe the column and row addresses into the eight address pins on a pair of TMS4464 DRAMs. Here, the RAS signal not only strobes the row address into the DRAMs, but it also selects which part of the address is applied to the address inputs. This is possible due to the long propagation-delay time of the multiplexers.

When $\overline{RAS}$ is a logic 1, the B inputs are connected to the Y outputs of the multiplexers; when the $\overline{RAS}$ input goes to a logic 0, the A inputs connect to the Y outputs. Because the internal row address latch is edge-triggered, it captures the row address before the address at the inputs changes to the column address.

As with the SRAM, the $R/\overline{W}$ pin writes data to the DRAM when logic 0, but there is no pin labeled G or enable. There also is no $\overline{S}$ (select) input to the DRAM. As mentioned, the input selects the DRAM. If selected, the DRAM is written if $R/\overline{W} = 0$ and read if $R/\overline{W} = 1$.



(a)

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

(b)

FIGURE 10–7 The pin-out of the TMS4464, 64K · 4 dynamic RAM (DRAM). (Courtesy of Texas Instruments Incorporated.)

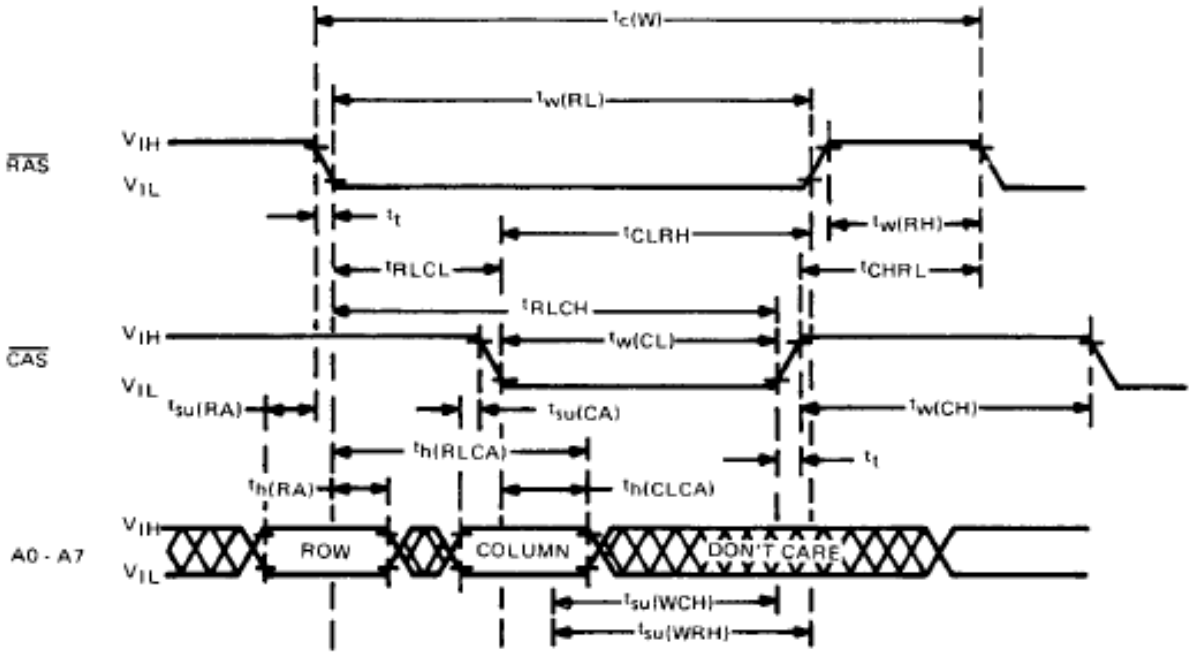


FIGURE 10–8 $\overline{RAS}$, $\overline{CAS}$, and address input timing for the TMS4464 DRAM. (Courtesy of Texas Instruments Incorporated.)

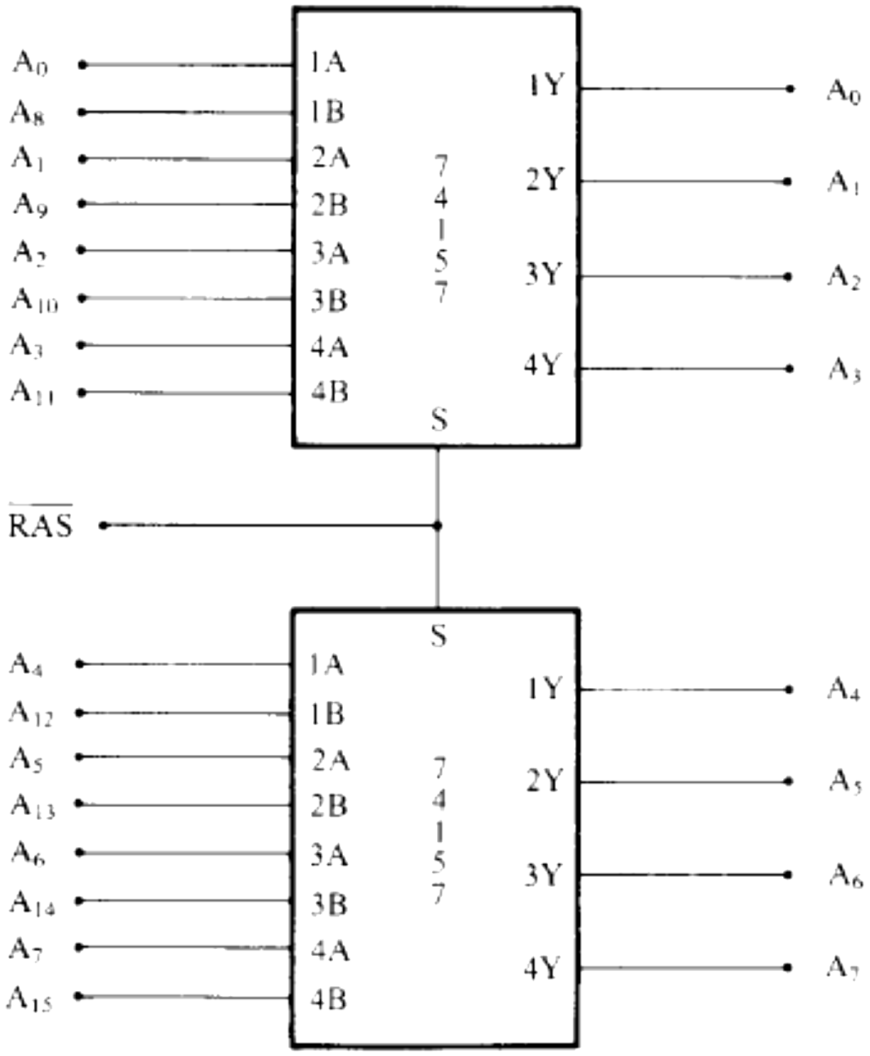
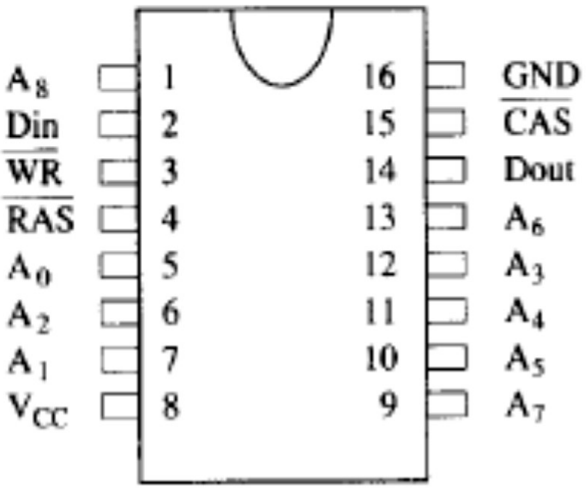


FIGURE 10–9 Address multiplexer for the TMS4464 DRAM.

Figure 10–10 shows the pin-out of the 41256 dynamic RAM. This device is organized as a 256K · 1 memory, requiring as little as 70 ns to access data. larger DRAMs have become available that are organized as a 16M · 1, 256M · 1, 512M · 1, 1G · 1, and 2G · 1 memory. On the horizon is the 4G · 1 memory, which is in the planning stages.



PIN FUNCTIONS

A_0 - A_8	Addresses
Din	Data in
Dout	Data out
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WR}$	Write enable
V_{CC}	+5V Supply
GND	Ground

FIGURE 10–10 The 41256 dynamic RAM organized as a 256K · 1 memory device.

The DIMM module is available in DRAM, EDO, SDRAM, and DDR (double-data rate) forms, Corporation, although this memory type has faded from the market. Like the SDRAM, the RIMM contains 168 pins, but each pin is a two-level pin, bringing the total number of Connections.
The fastest SDRAM currently available is the PC-4400 or 500 DDR, which operates at a rate of 4.4G bytes per second. By comparison, the 800 MHz RIMM operates at a rate of 3.2G bytes per second and is no longer supported in many systems. RDRAM had a fairly short life in the volatile computer market. The RIMM module is organized as a 32-bit-wide device. This means that to populate a Pentium 4 memory, RIMM memory is used in pairs. Intel claims that the Pentium 4 system using RIMM modules is 300% faster than a Pentium III using PC-100 memory.

According to RAMBUS, the current 800 MHz RIMM has been increased to a speed of 1200 MHz, but it is still not fast enough to garner much of a market share.

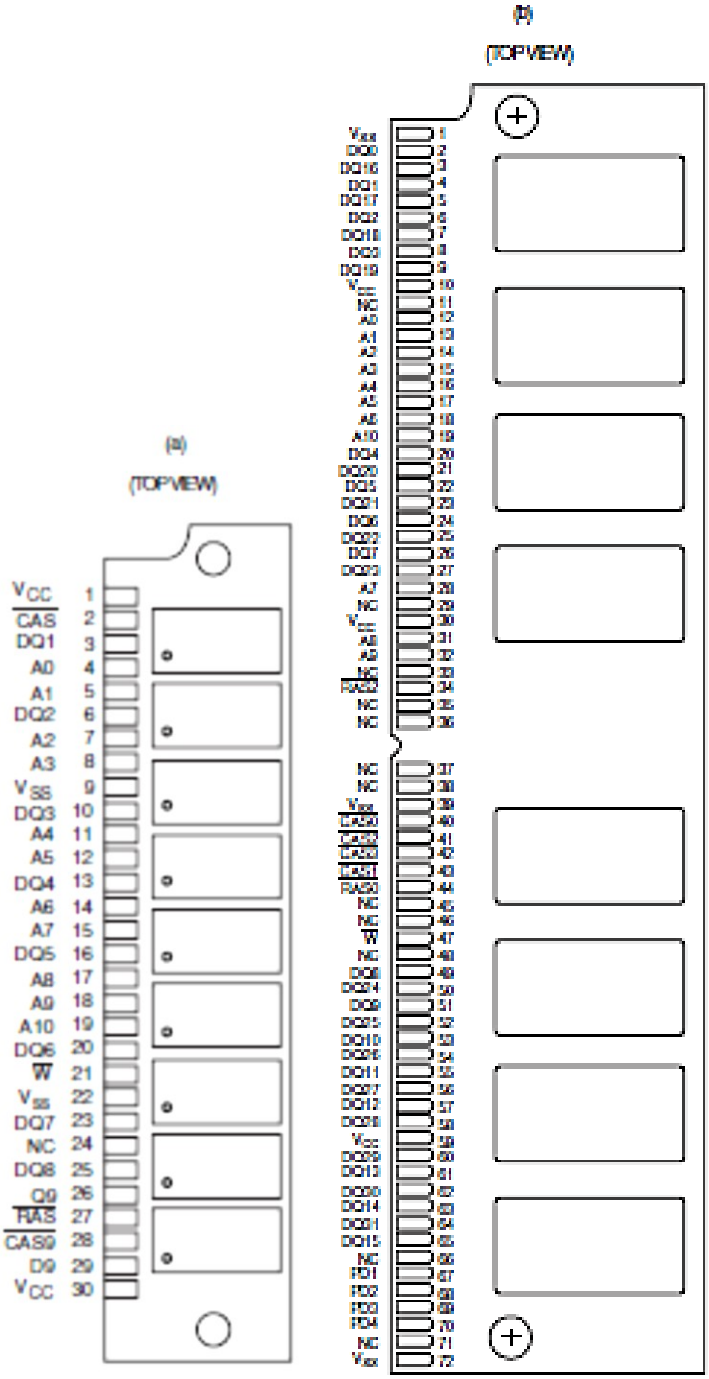


FIGURE 10–11 The pin-outs of the 30-pin and 72-pin SIMM. (a) A 30-pin SIMM organized as 4M · 9 and (b) a 72-pin SIMM organized as 4M · 36. to 336.