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* For the o/p c/cs, the active region exists to the right of the vertical dashed line at $V_{CE(sat)}$ and above the curve of I_B equal to zero. The region to the left of V_{CEsat} is called the saturation region.

* In the active region of a common-emitter amplifier, the base-emitter junction is forward-biased, whereas the collector-base junction is reverse-biased.

* we have $I_C = \alpha I_E + I_{CBO}$ equ (3-4)

$$I_C = \alpha (I_C + I_B) + I_{CBO} \quad \text{-----(3-5)}$$

Rearranging yields $I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$ ---(3-6)

for $I_B = 0$ $\quad I_C = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B=0} = I_{CEO}$ ---(3-7)

for $\alpha = 0.996$ and for $I_{CBO} = 1\mu A$

$I_{CEO} = 250\, I_{CBO} = 250\mu A$

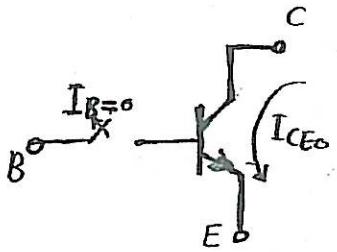

Fig (3-11) Circuit Condition related to I_{CEO}

* In dc mode

$$\beta_{dc} = \frac{I_C}{I_B} \quad \text{-------(3-8)}$$

(β ranges from about 50 to 400)

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = h_{fe} \quad \text{-------(3-9)}$$

(hybrid forward current gain for C.E)

* $I_E = I_C + I_B$

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$ (dividing path sides of equation by I_C)

$$\beta = \alpha\beta + \alpha = (\beta+1)\alpha$$

so that $\alpha = \frac{\beta}{\beta+1}$ -----(3-10)

or $\beta = \frac{\alpha}{1-\alpha}$ ---(3-11)

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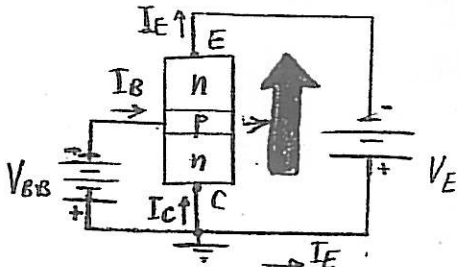
In addition, recall that $I_{CEo} = \frac{I_{CBo}}{1-\alpha}$ by using an equivalence of $\frac{1}{1-\alpha} = \beta + 1$ derived from the above, we find that

$$I_{CEo} = (\beta + 1)\, I_{CBo} \cong \beta\, I_{CBo} \qquad \text{---- (3-12)}$$

3-3) COMMON-COLLECTOR CONFIGURATION:

* The common-collector configuration is used primarily for impedance-matching since it has a high input impedance and low output impedance, opposite to that of C-B-C.



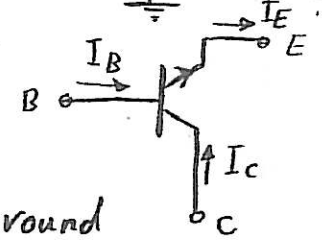


Fig (3-12)
Notation and symbol of common-collector configurat using npn transistor

* A C.C.C provided in Fig (3-13) with load resistor, with collector tied to ground even though the transistor is connected in amanner similar to C-E-C.

* The same o/p c/cs of C.E.C is used as $I_E \approx I_C$ versus V_{CE} for different values of I_B.

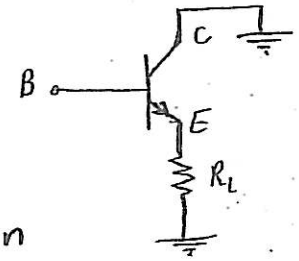


Fig (3-13)
C-C-C used for impedance matching

3-4 Limits of operation:

* For each transistor there is a region of operation on the c/cs that will ensure that the maximum ratings are not being exceeded and the output signal exhib minimum distortion.

limits V_{CEo} or $V_{(BR)CEo}$, I_{Cmax} and P_{Cmax} on a specification sheet of the transistor.

$P_{Cmax} = V_{CE}\, I_C$

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Chapter-4-

DC Biasing - BJTs

4-1) Introduction
4-2) Fixed-bias Circuit
4-3) Emitter Bias
4-4) DC Bias with voltage Feedback
4-5) Voltage-Divider Bias
4-6) Design Operations
4-7) Bias stabilization

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① Introduction:

* transistor can raise the level of the applied ac input without the assistance of an external energy source
* In actuality the improved output ac power level is the result of a transfer of energy from the applied dc supplies.
* DC biasing specifies desire dc current and voltage levels that will establish the desired operating point, and the design will determine the stability of the system, that is, how sensetive the system to temperature variation

* $V_{BE} = 0.7\ V$ — (4-1)

$I_E = (\beta + 1)\, I_B \cong I_C$ — (4-2)

$I_C = \beta I_B$ — (4-3)

* Since the operating point is a fixed point on the C/cs, it is called the quiescent point (abbreviated Q-point)

* Point B seems the best operating point in terms of linear gain and largest possible voltage and current swing.

* The maintenance of the operating point can be specified by a stability factor S, which indicates the degree of change in operating point due to a temperature variation, which vary β, I_{Co} and V_{BE}.

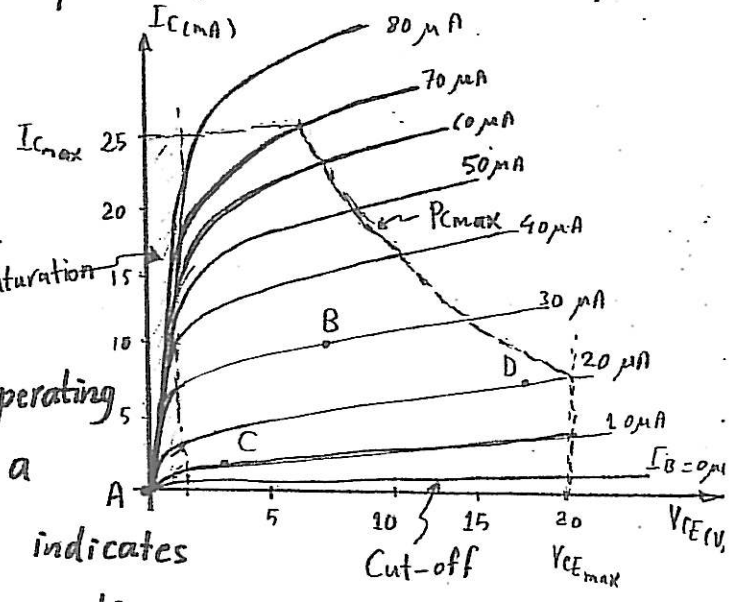

Fig (4-1)
Various operating points within the limits of operation of a transistor