② Fixed-bias Circuit:

* The fixed-bias circuit of Fig (4-2.)
* For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent.

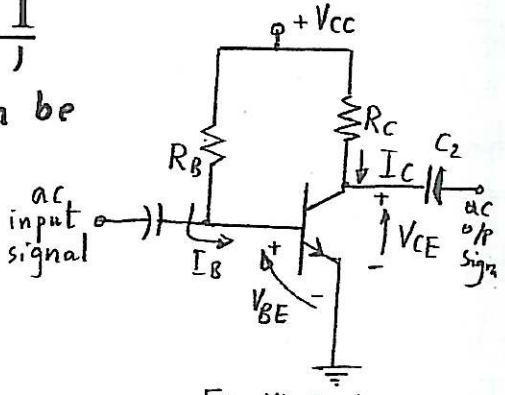


Fig (4-2) Fixed-bias circuit

* Forward bias of Base-Emitter writing kirchhoff's voltage equation in the clockwise direction

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad \text{---------- (4-4)}$$

* Collector-Emitter Loop

$$I_C = \beta I_B \qquad \text{---- (4-5)}$$

KVL applied clockwise direction

$$V_{CE} + I_C R_C - V_{CC} = 0 \qquad \text{---------- (4-6)}$$

$$V_{CE} = V_{CC} - I_C R_C \qquad \text{---------- (4-7)}$$

$$V_{CE} = V_C - V_E \qquad \text{---------- (4-8)}$$

$V_{CE} = V_C$ since $V_E = 0$

$$V_{BE} = V_B - V_E \qquad \text{---------- (4-9)}$$

$V_{BE} = V_B$ Since $V_E = 0$

* How the network parameters define the possible range of Q-points and how the actual Q-point is determined.

$$V_{CE} = V_{CC} - I_C R_C$$

on the output c/cs is to use the fact that astraight line is defined by two points.

set $I_C = 0$ so $V_{CE} = V_{CC}|_{I_C=0}$

set $V_{CE} = 0$ $I_C = \frac{V_{CC}}{R_C}\Big|_{V_{CE}=0}$

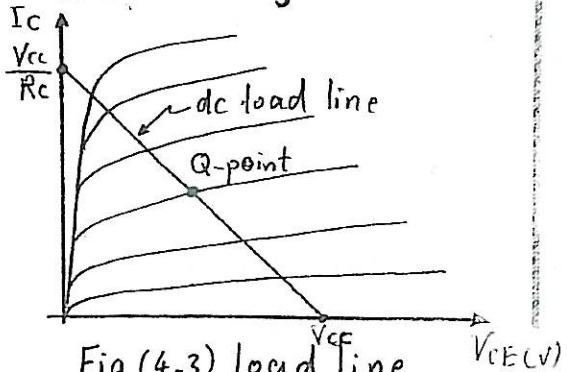


Fig (4-3) load line

③ Emitter Bias:

* It contains an emitter resistor to improve the stability level over that of the fixed-bias.

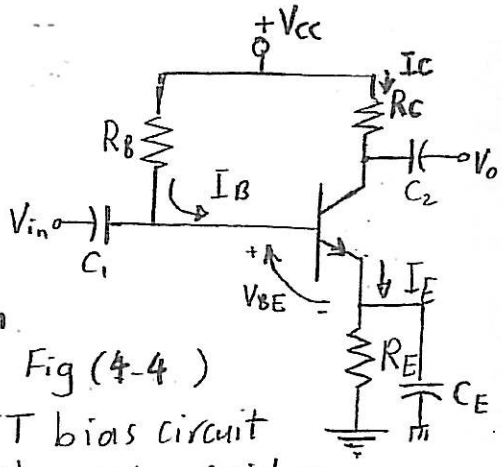


Fig (4-4)
BJT bias circuit with emitter resistor

* Base-Emitter Loop

KVL around i/p clockwise direction

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}} \quad \text{---------- (4-10)}$$

R_E reflected by $(\beta + 1)$ to the i/p resistance

* Collector-Emitter Loop

using KVL at o/p Loop clockwise direction results:

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

substituting $I_E \cong I_C$

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)} \quad \text{---------- (4-11)}$$

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

also $V_B = V_{CC} - I_B R_B$

$V_B = V_{BE} + V_E$

* and for d.c load line connected between

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}\Big|_{V_{CE}=0}$$

and $V_{CE} = V_{CC}\Big|_{I_C=0}$

Electronics I

* Set $R_C = R_L$

slope of ac load line $= -\frac{1}{R_L}$

$y - y_1 = m(x - x_1)$

$i_C - I_{CQ} = -\frac{1}{R_L}(V_{CE} - V_{CEQ})$

$i_{C\max}$ when $V_{CE} = 0$

$i_{C\max} = I_{CQ} + \frac{V_{CEQ}}{R_L}$

to obtain maximum symmetrical swing

$i_{C\max} = 2\, I_{CQ}$

$\frac{V_{CEQ}}{R_L} = I_{CQ}$

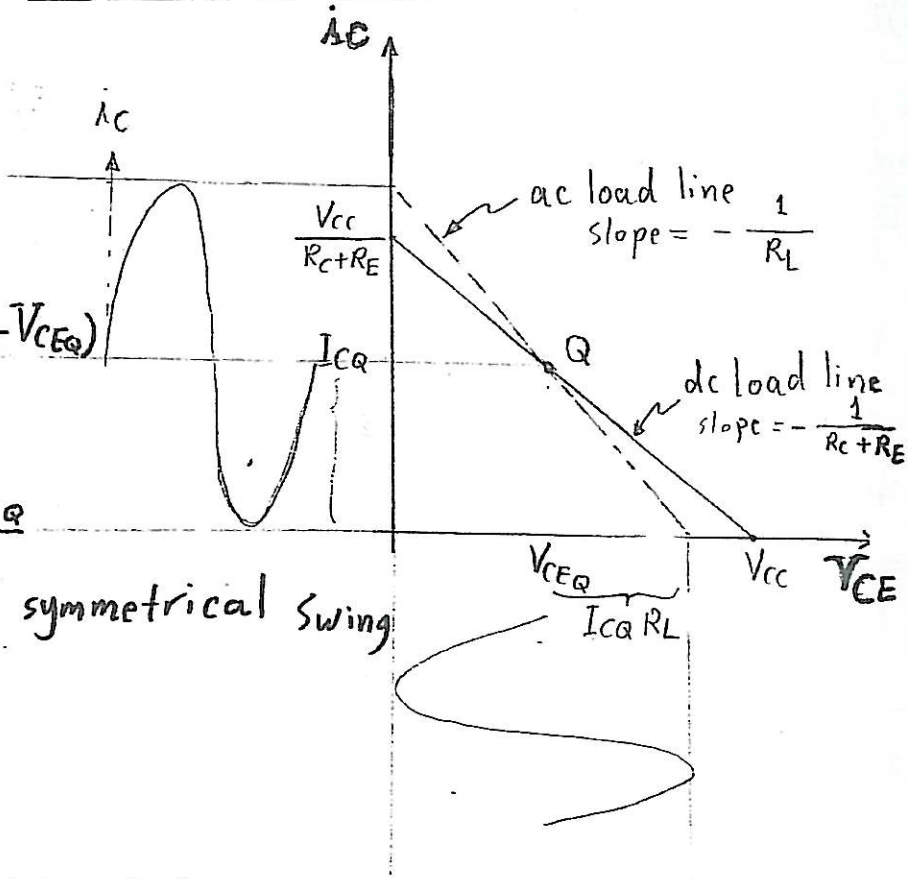


Fig (4-5) A

for d.c load line

$V_{CC} = V_{CEQ} + I_{CQ}(R_L + R_E)$

$V_{CC} = I_{CQ}R_L + I_{CQ}(R_L + R_E) = 2\, I_{CQ}R_L + I_{CQ}R_E$

$\therefore I_{CQ} = \frac{V_{CC}}{2R_L + R_E}$ for max. symmetrical swing

$R_{ac} = R_C = R_L$, $R_{d.c} = R_E + R_L$

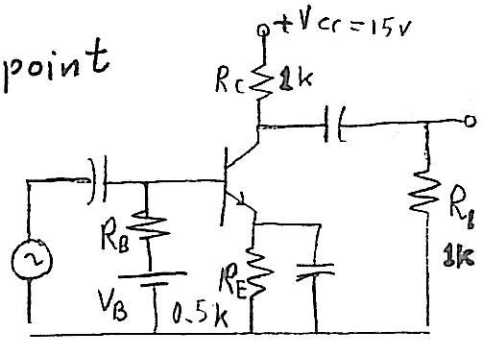
$$\boxed{I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}}}$$

$V_{CC} = V_{CEQ} + V_{CEQ} + \frac{V_{CEQ} * R_E}{R_L}$

$\therefore V_{CEQ} = \frac{V_{CC}}{2 + \frac{R_E}{R_L}} = \frac{V_{CC}}{1 + \frac{R_L}{R_L} + \frac{R_E}{R_L}} = \frac{V_{CC}}{1 + \frac{R_{dc}}{R_{ac}}}$

$$\therefore \boxed{V_{CEQ} = I_{CQ} * R_{ac}}$$

Ex: For the circuit shown, Find the Q-point for maximum symmetrical swing.



Ans: $I_{CQ} = 7.5\,mA$, $V_{CEQ} = 3.75V$

Electronics I

④ DC bias with Voltage feedback:

* An improved level of stability can be obtained by introducing a feedback path from collector to base as shown.

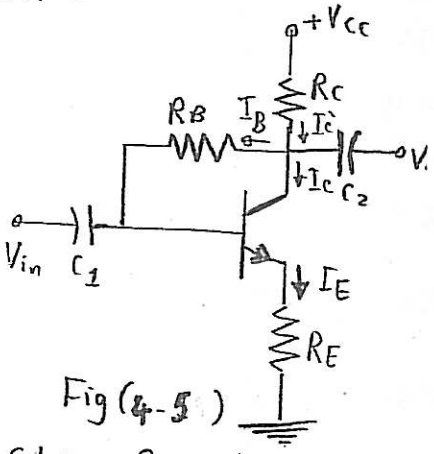


Fig (4-5) DC bias Circuit with voltage feedback

Base - Emitter Loop:

Writing KVL around clockwise direction

$$V_{CC} - I_C' R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$(I_C' = I_C + I_B) \approx I_C = \beta I_B$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)}} \quad \text{---- (4-12)}$$

* In general, the feedback path results in a reflection of the resistance R_C back to the input Circuit, much like the reflection of R_E.

Collector - Emitter Loop

$$I_E R_E + V_{CE} + I_C' R_C - V_{CC} = 0$$

Since $I_C' \cong I_C$ and $I_E \cong I_C$ we have

$$I_C (R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)} \quad \text{---- (4-13)}$$

⑤ VOLTAGE-DIVIDER BIAS: (β - independent)

* It is independent of β such a network

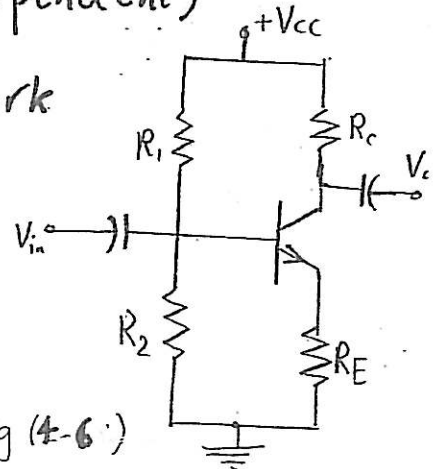


Fig (4-6) Voltage divider bias Configuration

Exact Analysis

The Thévenin equivalent network to the left of the base terminal can be found in following manner:

$$R_{th} = R_1 // R_2$$

$$E_{th} = V_{R_2} = V_{CC} * \frac{R_2}{R_1 + R_2}$$