* The Thévenin network is then redrawn as shown in Fig (4-7)

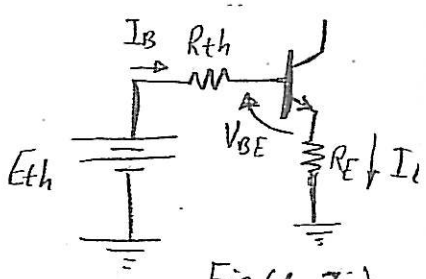

Fig (4-7)
Inserting the Thévenin equivalent circuit

$$E_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

substituting $I_E = (\beta + 1) I_B$

$$I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta+1) R_E} \qquad \text{---------- (4-14)}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \qquad \text{----- (4-15)}$$

Approximate Analysis

* The reflected resistance between base and emitter is defined by $R_i = (\beta + 1) R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 and I_2 will be approximately equal to I_1.

set $I_B = 0$, then $I_1 = I_2$, and R_1 and R_2 can be considered series elements.

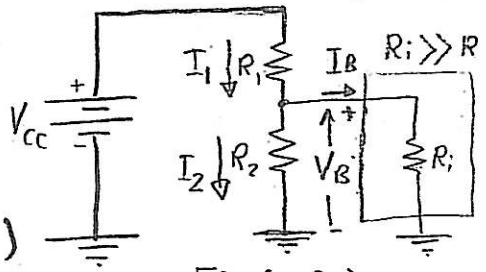

Fig (4-8)
Partial-bias circuit for calculating the approximate base voltage V_B.

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2} \qquad \text{------ (4-16)}$$

since $R_i = (\beta + 1) R_E \cong \beta R_E$

the condition that will define whether the approximate approach can be applied is :

$$\beta R_E \geq 10 R_2 \qquad \text{---------- (4-17)}$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

$$I_{CQ} \cong I_E$$

$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E)$$

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(6) Design operations:

* The design process is one where a current and voltage may be specified and the elements required to establish the designated levels must be determined.
* So for given I_{CQ} and V_{CEQ}, Determine R_1 and R_2, R_C and R_E for voltage divider circuit. (β given from C/cs)

$$V_E = I_E R_E \cong I_{CQ} R_E$$

take $V_E = \frac{1}{10} V_{CC}$ so $R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_{CQ}}$

$$R_C = \frac{V_{CC} - V_{CEQ} - V_E}{I_{CQ}}$$

$$V_B = V_{BE} + V_E$$

take $R_2 \leq \frac{1}{10} \beta R_E$

(7) BIAS STABILIZATION:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 2.5 mV per degree Celsius (°C) increase in temp

I_{CO}: (reverse saturation current): doubles in value for every 1° increase in temperature.

* Any or all of these factors can cause the bias point to drift from the designed point of operation.
* A stability factor S is defined for each of the parameter affecting bias stability as follows:

$$S_{(I_{CO})} = \frac{\Delta I_C}{\Delta I_{CO}}, \quad S_{(V_{BE})} = \frac{\Delta I_C}{\Delta V_{BE}}, \quad S_{(\beta)} = \frac{\Delta I_C}{\Delta \beta}$$

* The total effect on the collector current can be determined using the following equation:

$$\Delta I_C = S_{(I_{CO})} \Delta I_{CO} + S_{(V_{BE})} \Delta V_{BE} + S_{(\beta)} \Delta \beta$$

* The ratio $\frac{R_B}{R_E}$ or $\frac{R_{th}}{R_E}$ should be as small as possible with consideration to all aspects of the design including the ac response.

Electronics 1

Chapter - 5 -

AC Analysis of BJT

5-1) Introduction
5-2) BJT Transistor Modeling
5-3) The r_e Transistor Model
5-4) The Hybrid Equivalent Model
5-5) Hybrid π Model
5-6) Comon - Emitter Fixed - Bias Configuration
5-7) Voltage - Divicler Bias
5-8) CE Emitter - Bias Configuration
5-9) Emitter - Follower Configuration
5-10) Common - Base Configuration
5-11) Collector - Feedback Configuration
5-12) Effect of R_L and R_s
5-13) Cascadeed Systems
5-14) Darlington Connection

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Electronics 1

1) INTRODUCTION:

* Examine the ac response of BJT amplifier by reviewing the models most frequently used to represent the transistor in the sinusoidal ac domain.
* There are three models commonly used in the small-signal ac analysis: re model, the hybrid equivalent model and the hybrid-π model.
* Transistor can be employed as an amplifying device, the output ac power is greater than input ac power, as the dc power included in input.
* The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

2) BJT ~~Transistor~~ Models:

* A model is a combination of circuit elements, properly chosen, that best approximates the actual behaviour of a semiconductor device under specific operating conditions.
* To demonstrate the effect that the ac equivalent circuit will have on the analysis to follow the circuit of Fig (2-1).
* dc supplies can be replaced by a zero-potential equivalent (short circuit) as we interested on ac equivalent cct. In addition,

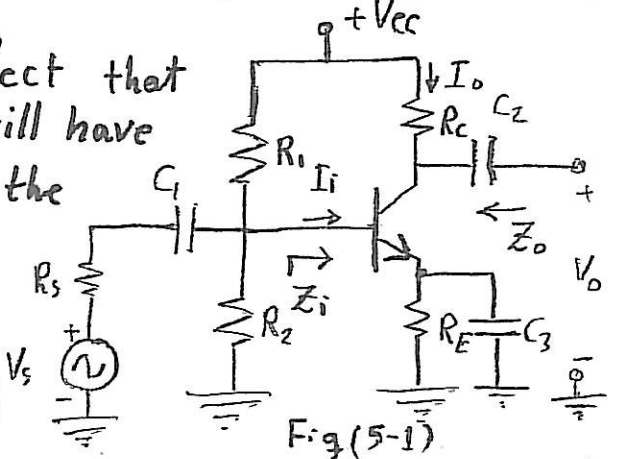

Fig (5-1)
Transistor Circuit under examination