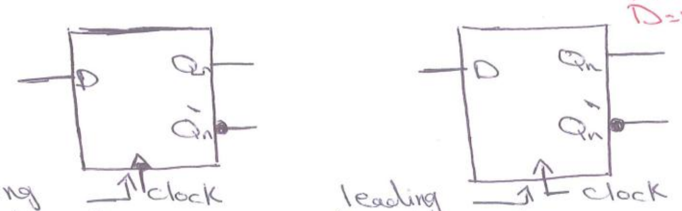
2- D F/F (Delay) flip-flop:-

It is the most economical and efficient flip-flop constructed because it requires the smallest number of gates. The name come from Delay, since the output is just the input delayed until the next active clock transition. Block diagram of D flip-flop, both trailling edge triggered and leading-edge triggered as shown below:-

Note:- $Q_{n+1} = D$
$D=0 \rightarrow Q_{n+1}=0$
$D=1 \rightarrow Q_{n+1}=1$



Trailing edge triggered   leading edge-triggered.

- Truth table, characteristic table and Excitation table for D f.f

Truth table

clk	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

clk = 1
characteristic table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

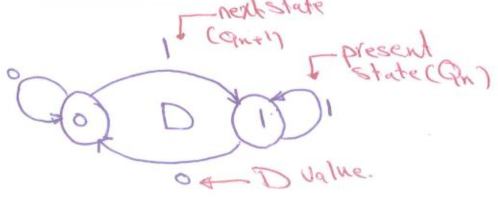
- characteristic equation and state diagram for D-ff are shown below:-

$Q_n \backslash D$	$\bar{D}$	D
$\bar{Q}_n$	0	1
Q_n	0	1

← from characteristic table

$$\boxed{Q_{n+1} = D}$$

← c/cs eq. of D.f.f.



state diagram for D f.f.

Solution:- By Comparing with J-K equation:-

$$Q_{n+1} = J_n \overline{Q}_n + \overline{K}_n Q_n$$

*Note:-

$Q_n = A_n$, B_n, C_n, D_n

$$A_{n+1} = \bar{A}\bar{B}CD + \bar{A}\bar{B}C + ACD + A\bar{C}\bar{D}$$

$$A_{n+1} = (\bar{B}CD + \bar{B}C)\bar{A} + (CD + \bar{C}\bar{D})A = (\bar{B}C[D+1])\bar{A} + (CD+\bar{C}\bar{D})A$$
$$= (\bar{B}C)\bar{A} + (CD+\bar{C}\bar{D})A$$

$$A_{n+1} = J_A \bar{A}_n + \bar{K}_A A_n$$

$\rightarrow J_A = \bar{B}\cdot C$

$\rightarrow \bar{K}_A = (CD + \bar{C}\bar{D}) \Rightarrow K_A = C\bar{D} + \bar{C}D$
$= C \oplus D$

$$B_{n+1} = \bar{A}C + C\bar{D} + \bar{A}B\bar{C}$$

$$B_{n+1} = (\bar{A}C + C\bar{D})(B+\bar{B}) + \bar{A}B\bar{C} \Rightarrow \bar{A}BC + BC\bar{D} + \bar{A}\bar{B}C + \bar{B}C\bar{D} + \bar{A}B\bar{C}$$

$$B_{n+1} = (\bar{A}C + C\bar{D})\bar{B} + (\bar{A}C + C\bar{D} + \bar{A}\bar{C})B$$

$$B_{n+1} = (\bar{A}C + C\bar{D})\bar{B} + [\bar{A}(C+\bar{C}) + C\bar{D}]B$$

$$B_{n+1} = (\bar{A}C + C\bar{D})\bar{B} + (\bar{A} + C\bar{D})B$$

$$B_{n+1} = J_B \bar{B}_n + \bar{K}_B B_n$$

$\rightarrow J_B = \bar{A}C + C\bar{D}$

$\rightarrow \bar{K}_B = \bar{A} + C\bar{D} \Rightarrow K_A = (A\cdot(\bar{C}+D))$
$= A\bar{C} + AD$

$$C_{n+1} = B$$

$$C_{n+1} = B(C_n + \bar{C}_n)$$

$$C_{n+1} = B\bar{C}_n + BC_n$$

$$C_{n+1} = J_C \bar{C}_n + \bar{K}_C C_n$$

$\rightarrow J_C = B$

$\rightarrow \bar{K}_C = B \Rightarrow K_C = \bar{B}$

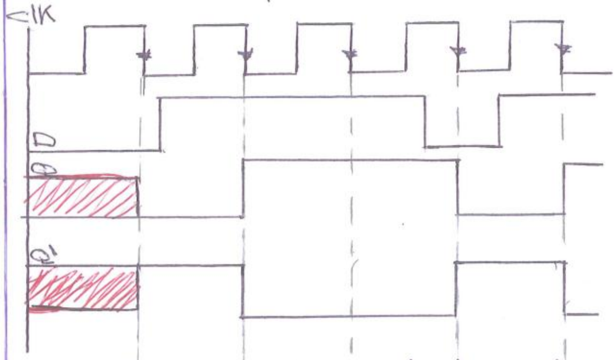
$$D_{n+1} = \bar{D}$$

$$D_{n+1} = J_D \bar{D}_n + \bar{K}_D D_n$$

$\rightarrow J_D = 1$

$\rightarrow \bar{K}_D = 0 \Rightarrow K_D = 1$

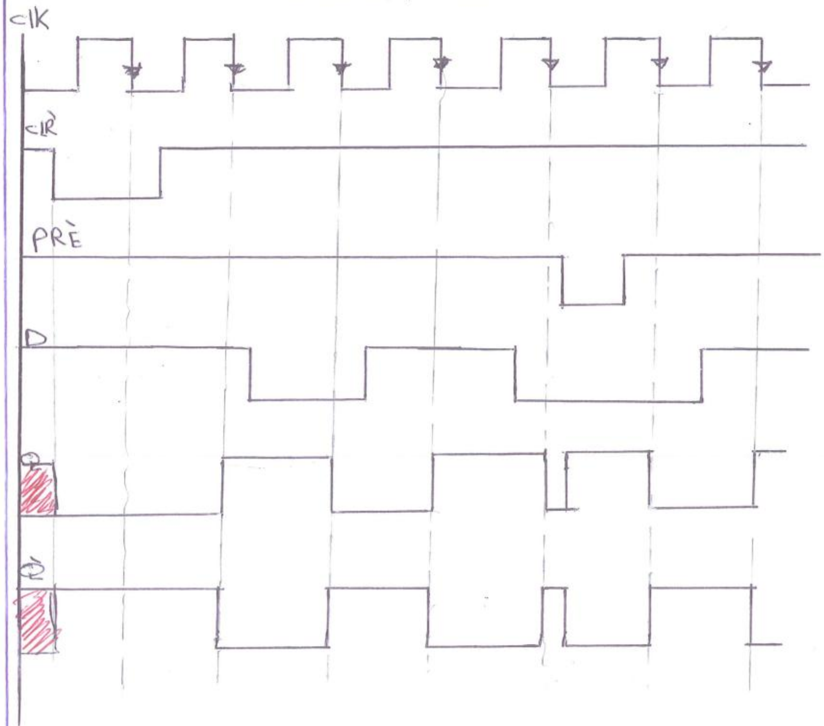
Example:- plot the output waveforms for the clock pulse and D flip-flop inputs shown below:-



*Note:- The behavior of The D flip-flop with $\overline{CLR}$ and $\overline{PRE}$ inputs is described by the truth tabel below:-

$\overline{CLR}$	$\overline{PRE}$	D	Q_{n+1}
0	0	X	X
0	1	X	0
1	0	X	1
1	1	0	0
1	1	1	1

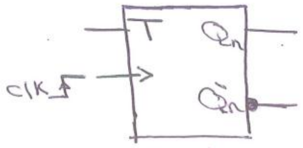
Example:- plot the output waveforms for D-flip-flop with clear and preset inputs:-



H.W:- Repeat the above plot waveforms with leading edge triggered (positive response) edge triggered.

3- T f/f (Toggle) flip-flop:-

It has one input, T, such that if T=1, the flip-flop changes state (that is, is toggled), and if T=0, the state remains the same. The block diagram of T flip flop with +ve going edge is shown below:-



T flip-flop
with +ve going edge

Note:-
memory state ← $T=0$; $Q_{n+1}=Q_n$
toggle state ← $T=1$, $Q_{n+1}=\bar{Q}_n$

- Truth table, characteristic table and Excitation table for T f.f.:-

Truth table

clk	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\bar{Q}_n$

clk = 1
characteristic table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

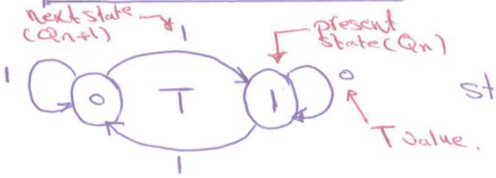
- characteristic equation and state diagram for T flip-flop:-

Q_n \ T	$\bar{T}$	T
$\bar{Q}_n$	0	1
Q_n	1	0

← from charactristic table

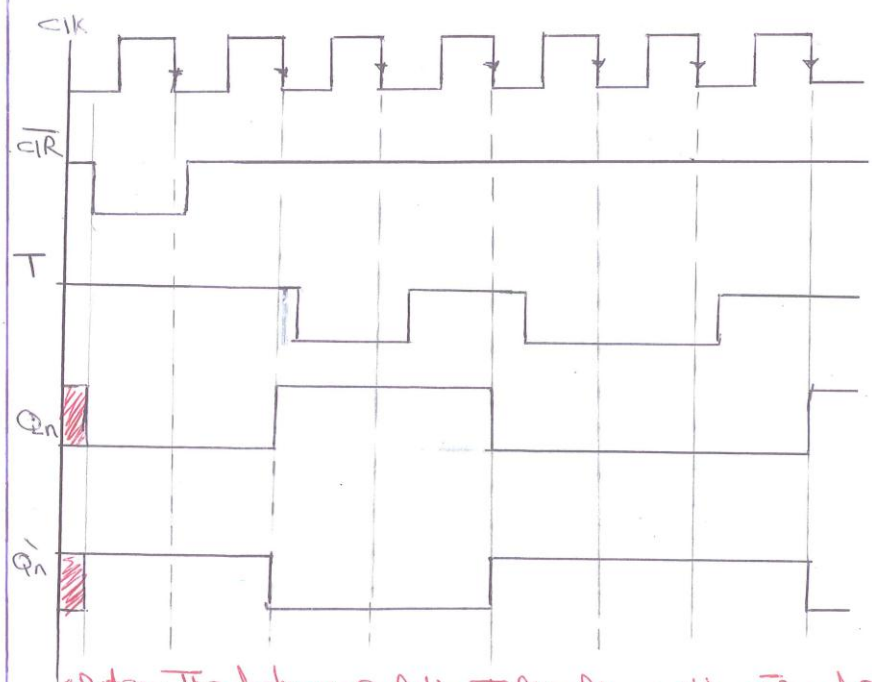
$$\boxed{\begin{aligned} Q_{n+1} &= T\bar{Q}_n + \bar{T}Q_n \\ &= T \oplus Q_n \end{aligned}}$$

← c/cs equation of T.f.f.



state diagram for T.f.f

Example:- plot the output waveforms for the clock pulse, $\overline{CLR}$ and T flip-flop inputs shown below:-

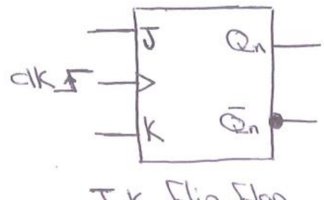


*Note:- The behavior of the T flip flop with $\overline{ClR}$ and $\overline{PRE}$ inputs is described by the truth table:-

$\overline{ClR}$	$\overline{PRE}$	T	Q_{n+1}
0	0	X	X
0	1	X	0
1	0	X	1
1	1	0	Q_n
1	1	1	$\overline{Q_n}$

4- J-K flip flop :-

It is a combination of the SR and T flip-flops, in that it behaves like an SR flip-flop, except that ($J=K=1$) causes the flip-flop to change state (as $T=1$). The block diagram of J-K flip-flop with +ve going edge is shown below:-



J-K flip-flop with +ve going edge.

Note:-

behave as SR f.f
- $J=K=0 \rightarrow Q_{n+1}=Q_n$
- $J=0, K=1 \rightarrow Q_{n+1}=0$
- $J=1, K=0 \rightarrow Q_{n+1}=1$

behave as T f.f in Toggle state.
- $J=K=1 \rightarrow Q_{n+1}=\bar{Q}_n$

- Truth table, characteristic table and Excitation table for J-K f.f :-

Truth table

clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

clk=1
characteristic table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation table

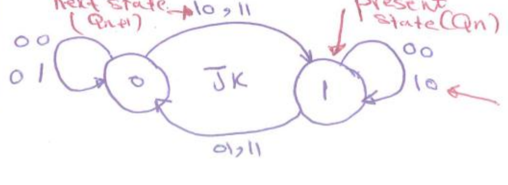
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- characteristic equation and state diagram for J-K flip-flop:-

Q_n \ JK	$\bar{J}\bar{K}$	$\bar{J}K$	JK	$J\bar{K}$
$\bar{Q}_n$	0	0	1	1
Q_n	1	0	0	1

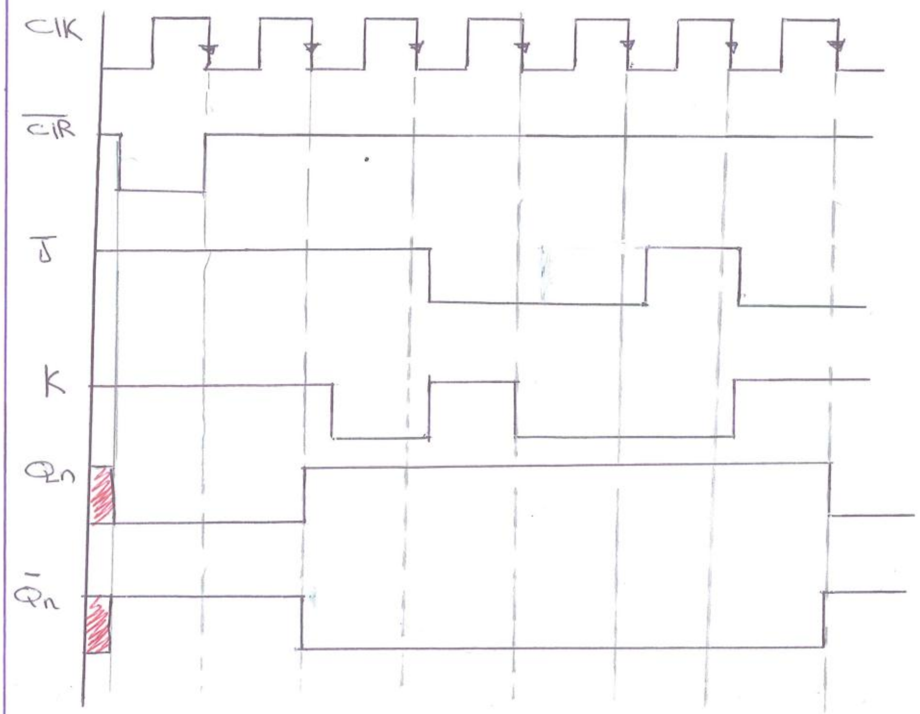
← from characteristic table

$$\boxed{Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n}$$ ← C/cs eq. for J-K flip-flop.



state diagram for J-K flip-flop

Example:- plot the output waveforms for the clock pulse, $\overline{CLR}$ and J-K flip-flop inputs shown below:- (103)



Note:- The behavior of the J-K flip-flop with $\overline{ClR}$ and $\overline{PRE}$ inputs is described by the truth table below:-

$\overline{ClR}$	$\overline{PRE}$	J	K	Q_{n+1}
0	0	X	X	X
0	1	X	X	0
1	0	X	X	1
1	1	0	0	Q_n
1	1	0	1	0
1	1	1	0	1
1	1	1	1	$\overline{Q}_n$