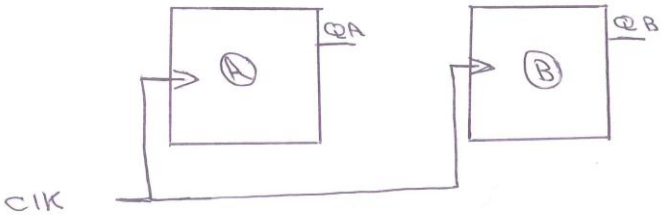
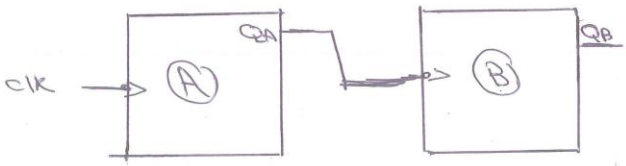
- Counters:-

Counters are classified into two broad catagories according to the way they are clocked:-

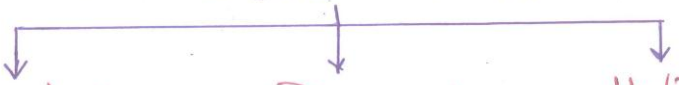
1- **Synchronous Counters:-** The clock input is Connected to all of the Flip-flops; so that they are clocked simultaneously.



2- **Asynchronous (Ripple) Counters:-** The first Flip-Flop is clocked by external clock pulse and then each successive Flip-flop is clocked by the output of the preceding Flip-Flop:-



- Types of Counters (Synchronous, Asynchronous):-



Up Counter (0-1-2-3-...)

Down Counter (7,6,5---0)

Up/Down counter
* Need control input

- Synchronous Counter operation:-

Design of synchronous Counter:-

1- Decide the number of flip-flops.

2- State diagram.

3- Flip-Flop Transition table (Circuit excitation table).

4- obtain simplified equations using K-maps.

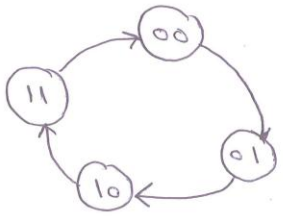
5- Draw the logic Diagram (Counter implementation).

Example:- Design mod4 (0 → 3) synchronous Counter using SR Flip-Flop.

Solution:- 0 → 1 → 2 → 3

No. of bits = 2 = No. of Flip-Flops.

Present state B_n	Present state A_n	Next state B_{n+1}	Next state A_{n+1}	S_B	R_B	S_A	R_A
0	0	0	1	0	d	1	0
0	1	1	0	1	0	0	1
1	0	1	1	d	0	1	0
1	1	0	0	0	1	0	1



State diagram

A \ B	$\bar{B}$	B
$\bar{A}$	0	d
A	1	0

$S_B = \bar{B}A$

A \ B	$\bar{B}$	B
$\bar{A}$	d	0
A	0	1

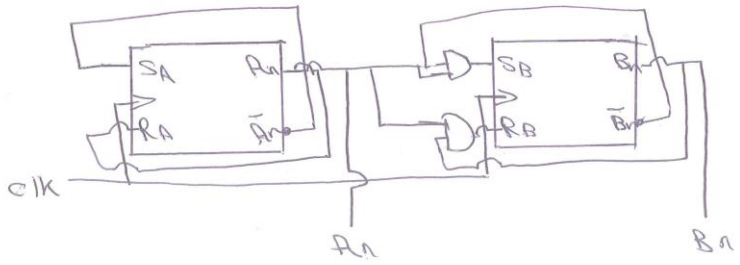
$R_B = BA$

A \ B	$\bar{B}$	B
$\bar{A}$	1	1
A	0	0

$S_A = \bar{A}$

A \ B	$\bar{B}$	B
$\bar{A}$	0	0
A	1	1

$R_A = A$

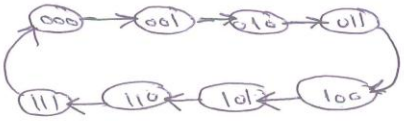


Example:- Design mod 8 (0 → 7) synchronous counter using JK-Flip-Flop.

*Note:- (up counter)

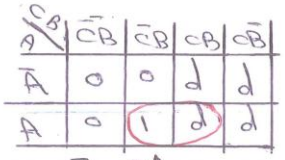
Solution:- 0 → 1 → 2 → 3 → 4 → 5 → 6 → 7

No. of bits = 3
= No. of flip-flops.

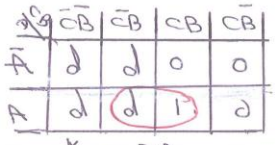


state-diagram.

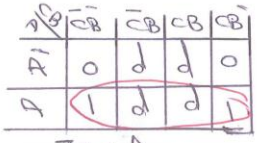
present state C_n B_n A_n	next state C_{n+1} B_{n+1} A_{n+1}	J_C K_C	J_B K_B	J_A K_A
0 0 0	0 0 1	0 d	0 d	1 d
0 0 1	0 1 0	0 d	1 d	d 1
0 1 0	0 1 1	0 d	d 0	1 d
0 1 1	1 0 0	1 d	d 1	d 1
1 0 0	1 0 1	d 0	0 d	1 d
1 0 1	1 1 0	d 0	1 d	d 1
1 1 0	1 1 1	d 0	d 0	1 d
1 1 1	0 0 0	d 1	d 1	d 1



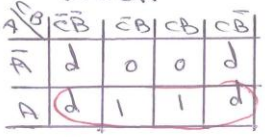
$J_C = BA$



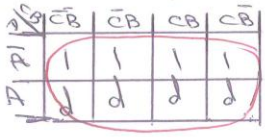
$K_C = BA$



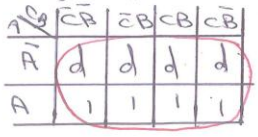
$J_B = A$



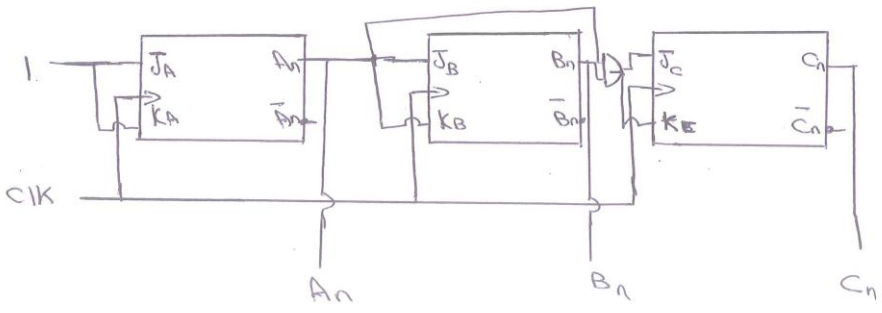
$K_B = A$



$J_A = 1$



$K_A = 1$



H-w Repeat the previouse Example using (SR) - D-T Flip-flop

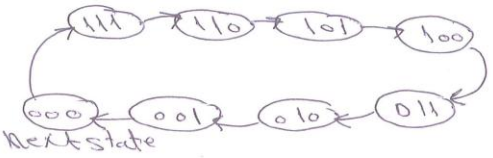
Example: Design a counter with the following binary sequence

$7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0$

using D-Flip-Flop:-

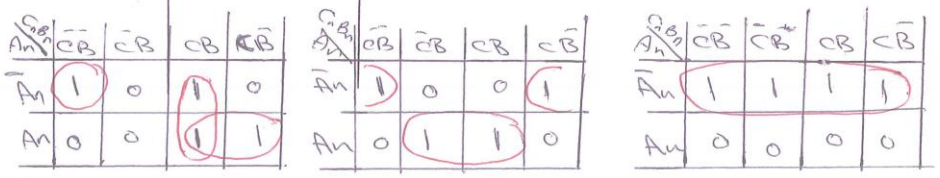
*Note:- Down counter

Solution:- no. of bits = 3 = no. of Flip-flops

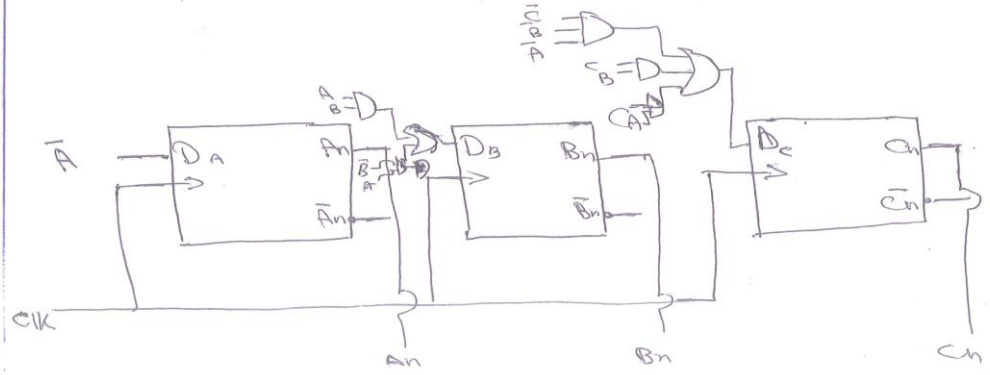


state diagram

C_n	B_n	A_n	C_{n+1}	B_{n+1}	A_{n+1}	D_C	D_B	D_A
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1
0	1	1	0	1	0	0	1	0
1	0	0	0	1	1	0	1	1
1	0	1	1	0	0	1	0	0
1	1	0	1	0	1	1	0	1
1	1	1	1	1	0	1	1	0



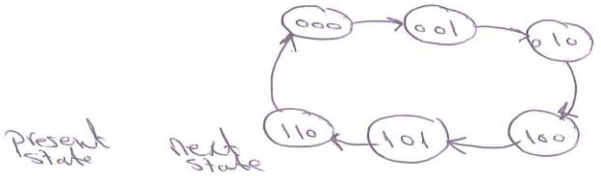
$D_C = \bar{C}\bar{B}\bar{A} + CB + CA_n$ $D_B = \bar{B}A + B\bar{A}$ $D_A = \bar{A}$



H.w: Design a Counter with the following binary sequence 0, 3, 2, 4, 1, 6, 5, 7 and repeat using D F.F.

Example:- Design a synchronous counter that has a repeated sequences of six states 0, 1, 2, 4, 5, 6, using JK Flip-Flop.

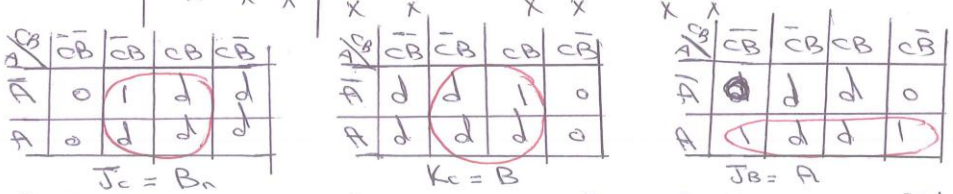
Solution:- no. of bits = 3 = no. of flip-flop.

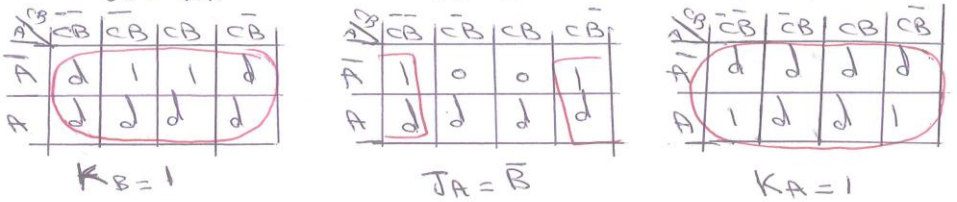


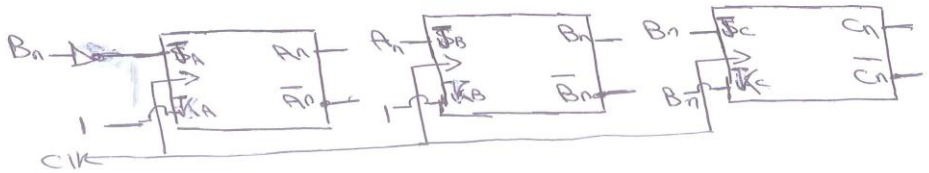
State diagram

Present State | Next State

C_n	B_n	A_n	C_{n+1}	B_{n+1}	A_{n+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	d	0	d	1	d
0	0	1	0	1	0	0	d	1	d	d	1
0	1	0	1	0	0	1	d	d	1	0	d
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	1	0	1	d	0	0	d	1	d
1	0	1	1	1	0	d	0	1	d	d	1
1	1	0	0	0	0	d	1	d	1	0	d
1	1	1	X	X	X	X	X	X	X	X	X

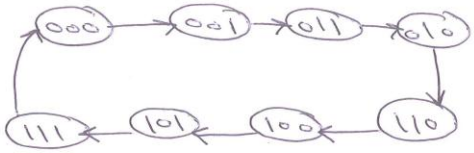






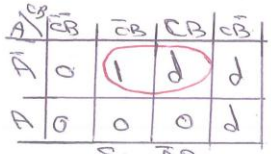
Example:- Design a Counter with the following Binary Sequence 0, 1, 3, 2, 6, 4, 5, 7 and repeat, using SR Flip-Flop.

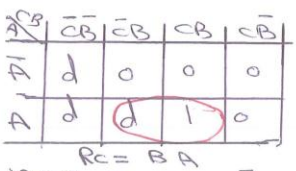
Solution:- No. of bits = 3 = No. of flip-flops

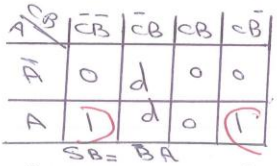


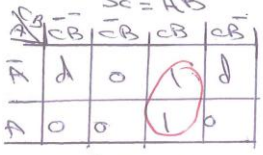
State diagram

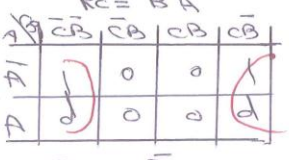
C_n B_n A_n	C_{n+1} B_{n+1} A_{n+1}	S_C R_C	S_B R_B	S_A R_A
0 0 0	0 0 1	0 d	0 d	1 0
0 0 1	0 1 1	0 d	1 0	d 0
0 1 0	1 1 0	1 0	d 0	0 d
0 1 1	0 1 0	0 d	d 0	0 1
1 0 0	1 0 1	d 0	0 d	1 0
1 0 1	1 1 1	d 0	1 0	d 0
1 1 0	1 0 0	d 0	0 1	0 d
1 1 1	0 0 0	0 1	0 1	0 1

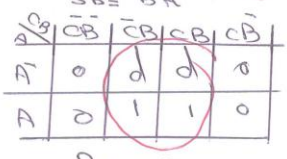

$S_C = \bar{A}B$


$R_C = BA$


$S_B = BA$


$R_B = \bar{C}B$


$S_A = \bar{B}$


$R_A = B$