

H.w:- Design the counter with the sequence 0, 3, 2, 4, 1, 5, 7 and repeat using D-Flip-flop.

H.w:- Design a counter that goes the sequence (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, ...) using D-Flip-flop.

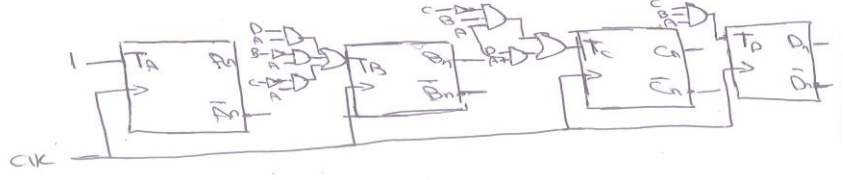
Example:- Design a synchronous counter that counts the decimal digits according to the 2421 codes using T-Flip-flop.

Solution:- decimal digit: 0 → 9  
 present state      No. of bits = 4 = No. of Flip-flops.  
 next state

D <sub>3</sub>	C <sub>4</sub>	B <sub>2</sub>	A <sub>1</sub>	D <sub>3</sub>	C <sub>4</sub>	B <sub>2</sub>	A <sub>1</sub>	T <sub>D</sub>	T <sub>C</sub>	T <sub>B</sub>	T <sub>A</sub>
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	1	0	0	1	1
0	0	1	1	0	0	1	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	1	0	1	1	1	0	0	0	1
1	1	1	0	1	1	1	0	1	0	0	1
1	1	1	1	1	1	1	1	0	0	0	1

$\frac{B}{A}$	$\overline{D}$	$\overline{C}$	$\overline{D}$	$\overline{C}$	$\frac{B}{A}$	$\overline{D}$	$\overline{C}$	$\overline{D}$	$\overline{C}$	$\frac{B}{A}$	$\overline{D}$	$\overline{C}$	$\overline{D}$	$\overline{C}$
$\overline{B}$	0	0	X	X	$\overline{B}$	0	0	X	X	$\overline{B}$	1	1	X	X
B	0	0	X	X	$\overline{B}$	0	0	X	X	B	1	1	X	X
B	0	1	1	X	B	0	1	1	X	B	1	1	1	X
$\overline{B}$	0	0	0	X	$\overline{B}$	0	0	0	X	$\overline{B}$	1	1	1	X

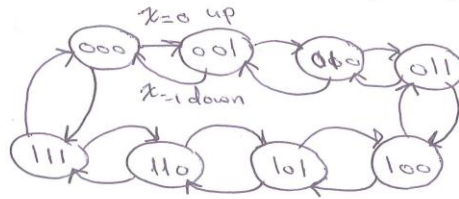
$T_D = CBA$        $T_C = DA + \overline{C}BA$        $T_B = DA + BA + \overline{C}A$        $T_A = 1$



Example:- Design a 3-bit synchronous counter, the counter counts up when the external input  $X=0$  and down when  $X=1$ , using T flip-flop:-

Solution:- No. of bits = 3 = No. of flip-flops.

note:- up/down counter  
 $X=0$  up  
 $X=1$  down



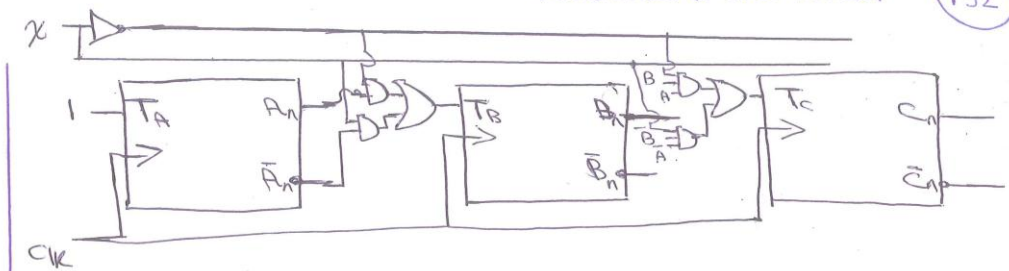
input	X	Cn	Bn	An	Cn-1	Bn-1	An-1	Tc	Tb	Ta
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0
0	0	0	1	0	0	1	1	0	0	0
0	0	0	1	1	1	0	0	0	0	0
0	0	1	0	0	1	0	1	0	0	0
0	0	1	0	1	1	1	0	0	0	0
0	0	1	1	0	0	1	1	0	0	0
0	0	1	1	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0	0
1	1	0	1	1	0	0	1	0	0	0
1	1	1	0	0	0	0	1	0	0	0
1	1	1	0	1	0	0	1	0	0	0
1	1	1	1	0	0	0	1	0	0	0
1	1	1	1	1	0	0	1	0	0	0

$\frac{Q_n}{Q_{n-1}}$	$\bar{X}_c$	$\bar{X}_c$	$X_c$	$X_c$	$\frac{Q_n}{Q_{n-1}}$	$\bar{X}_c$	$\bar{X}_c$	$X_c$	$X_c$	$\frac{Q_n}{Q_{n-1}}$	$\bar{X}_c$	$\bar{X}_c$	$X_c$	$X_c$
$\bar{B}_A$	0	0	0	1	$\bar{B}_A$	0	0	0	1	$\bar{B}_A$	1	1	1	1
$B_A$	0	0	0	0	$\bar{B}_A$	1	1	0	0	$B_A$	1	1	1	1
$B_A$	1	1	0	0	$B_A$	1	1	0	0	$B_A$	1	1	1	1
$B\bar{A}$	0	0	0	0	$B\bar{A}$	0	0	1	1	$B\bar{A}$	1	1	1	1

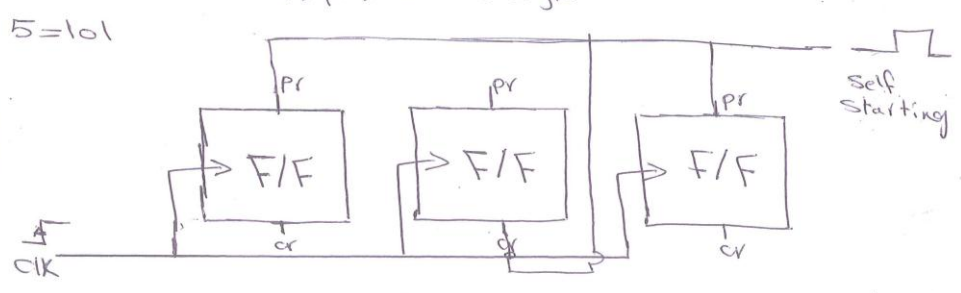
$T_c = \bar{X}BA + X\bar{B}\bar{A}$      
 $T_b = \bar{X}A + X\bar{A}$      
 $T_a = 1$



Properties of Synchronous Counter:-

1. Self Starting:- This property used to starting the counter on the desired initial state by counting an external line to (Pr, Cr) lines in the counter.

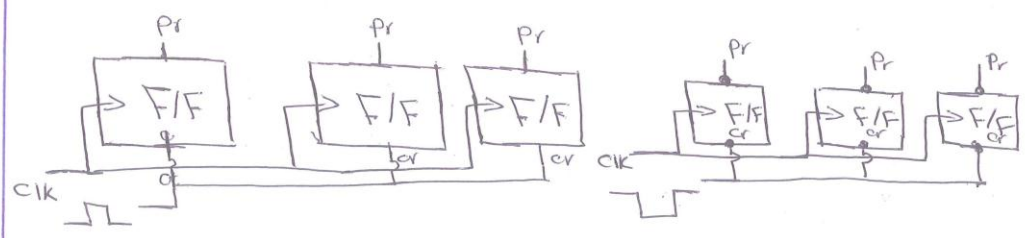
Example:- the counter has the property of self starting from (5) (Cr, pr) active high.



Example:- Draw the block diagram for a counter (3-bit) with self clearing (Zero self starting):-

- ① active high (Cr, pr).
- ② active low (Cr, pr).

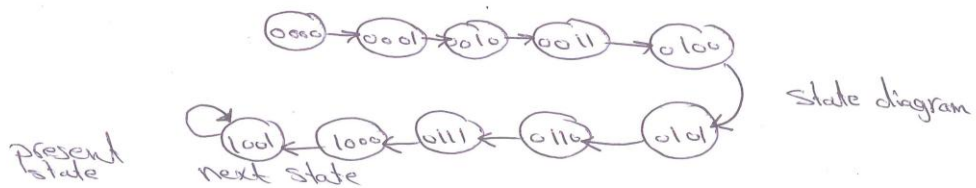
Solution:- 1- active high (Cr, pr)      2- active low (Cr, pr).



2. Self stopping (Dead end):- This property used to stop the counter on the desired state. This self stopping property can be obtained by the state table and putting the next state as the same as present state (desired stopping state).

Example:- Design BCD up synchronous counter with the property of self stopping using D Flip-flop

Solution:- no. of bits = 4 = no. of Flip-flop



Present state	Next state	D <sub>a</sub>	D <sub>b</sub>	D <sub>c</sub>	D <sub>d</sub>
0000	0001	0	0	0	1
0001	0010	0	0	1	0
0010	0011	0	0	1	1
0011	0100	0	1	0	0
0100	0101	0	1	1	0
0101	0110	0	1	1	1
0110	0111	1	0	0	0
0111	1000	1	0	0	1
1000	1001	1	0	0	1
1001	1001	X	X	X	X
1010	X	X	X	X	X
1011	X	X	X	X	X
1100	X	X	X	X	X
1101	X	X	X	X	X
1110	X	X	X	X	X
1111	X	X	X	X	X

$\frac{D}{C} \backslash \frac{B}{A}$	$\bar{D}\bar{C}$	$\bar{D}C$	$D\bar{C}$	$DC$
$\bar{B}\bar{A}$	0	0	X	1
$\bar{B}A$	0	0	X	1
$B\bar{A}$	0	1	X	X
$B\bar{A}$	0	0	X	X

$D_D = D + CBA$

$\frac{D}{C} \backslash \frac{B}{A}$	$\bar{D}\bar{C}$	$\bar{D}C$	$D\bar{C}$	$DC$
$\bar{B}\bar{A}$	0	1	X	0
$\bar{B}A$	0	1	X	0
$B\bar{A}$	1	0	X	X
$B\bar{A}$	0	1	X	X

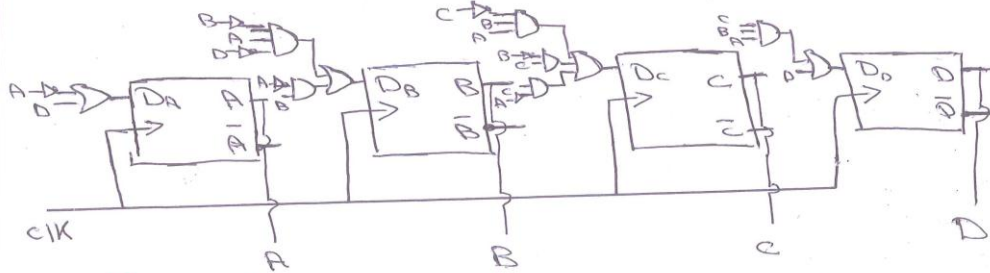
$D_C = \bar{B}A + C\bar{A} + \bar{B}C$

$\frac{D}{C} \backslash \frac{B}{A}$	$\bar{D}\bar{C}$	$\bar{D}C$	$D\bar{C}$	$DC$
$\bar{B}\bar{A}$	0	0	X	0
$\bar{B}A$	1	1	X	0
$B\bar{A}$	0	0	X	X
$B\bar{A}$	1	1	X	X

$D_B = \bar{B}\bar{A} + \bar{B}A\bar{D}$

$\frac{D}{C} \backslash \frac{B}{A}$	$\bar{D}\bar{C}$	$\bar{D}C$	$D\bar{C}$	$DC$
$\bar{B}\bar{A}$	1	1	X	1
$\bar{B}A$	0	0	X	1
$B\bar{A}$	0	0	X	X
$B\bar{A}$	1	1	X	X

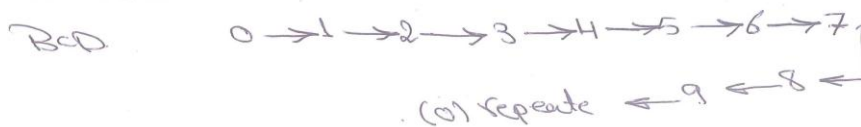
$D_A = \bar{A} + D$



3- Self correction: - This property used to avoid an error states (unwanted states). It can be obtained by putting initial state in the unwanted state instead of don't care conditions in the state table.

Example: - Design BCD up synchronous counter that has the property of self correction using D- flip-flop.

Solution: - no. of bits = 4 = no. of flip-flop.



$D_n$	$C_n$	$B_n$	$A_n$	$D_{n-1}$	$C_{n-1}$	$B_{n-1}$	$A_{n-1}$	$D_n$	$D_c$	$D_b$	$D_a$
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	0
0	0	1	1	0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	0	0	1	0	0
0	1	0	1	0	0	1	0	0	1	0	0
0	1	1	0	0	0	1	1	0	0	1	0
0	1	1	1	0	0	1	1	0	0	1	0
1	0	0	0	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	0	0	0	0	1	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0

$D_n$	$D_c$	$D_b$	$D_a$
$\bar{B}\bar{A}$	0	0	1
$B\bar{A}$	0	0	0
$B\bar{A}$	0	1	0
$B\bar{A}$	0	0	0

$D_b = \bar{D}CBA + D\bar{C}B\bar{A}$

$D_n$	$D_c$	$D_c$	$D_c$
$\bar{B}\bar{A}$	0	1	0
$B\bar{A}$	0	1	0
$B\bar{A}$	1	0	0
$B\bar{A}$	0	1	0

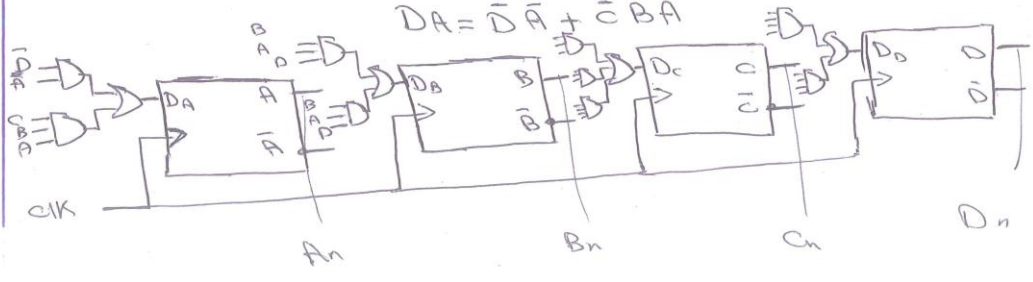
$D_c = \bar{D}C\bar{B} + \bar{D}C\bar{A} + D\bar{C}B\bar{A}$

$D_n$	$D_c$	$D_c$	$D_c$
$\bar{B}\bar{A}$	0	0	0
$B\bar{A}$	1	1	0
$B\bar{A}$	0	0	0
$B\bar{A}$	1	1	0

$D_B = \bar{B}A\bar{B}A\bar{D}$

$D_n$	$D_c$	$D_c$	$D_c$
$\bar{B}\bar{A}$	1	1	0
$B\bar{A}$	0	0	0
$B\bar{A}$	0	0	0
$B\bar{A}$	1	1	0

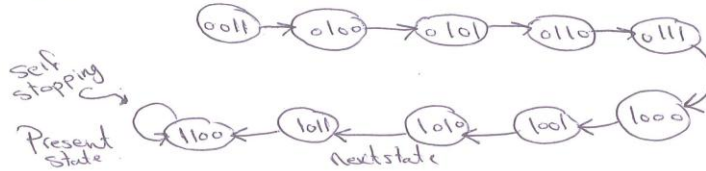
$D_A = \bar{D}\bar{A} + \bar{C}\bar{B}\bar{A}$



Example:- Design an Ex-3 synchronous up <sup>counter</sup> has the property of self stopping and self correcting to initial state using D.F.F.

Solution:- no. of bits = 4 = no. of Flip-Flop

0, 1, 2, 13, 14, 15 → self correcting.



$D_A$	$C_n$	$B_n$	$A_n$	$D_{n+1}$	$C_{n+1}$	$B_{n+1}$	$A_{n+1}$	$D_n$	$D_c$	$D_B$	$D_A$
0	0	0	0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	1	1	0	0	1	1
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	1	0
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	0	0
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	0
1	0	1	1	1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	0	1	1	0	0
1	1	0	1	0	0	1	1	0	0	1	1
1	1	1	0	0	0	1	1	0	0	1	1
1	1	1	1	0	0	1	1	0	0	1	1

H.w:- Find the equ. for  $D_B$ ,  $D_C$ ,  $D_B$  &  $D_A$  using X-map and then connect the ccb.

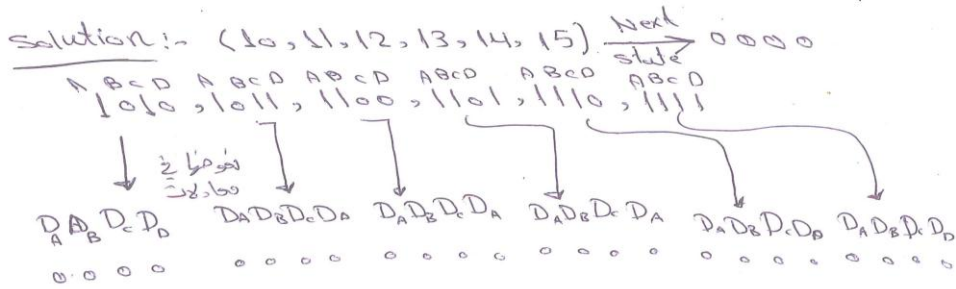
Example :- Check if the following system has the property of self correcting, with the BCD up synchronous Counter that has the following state equation :-

$$D_A = A\bar{B}\bar{C}\bar{D} + \bar{A}BCD \text{ (MSB)}$$

$$D_B = \bar{A}B\bar{D} + \bar{A}B\bar{C} + \bar{A}\bar{B}CD$$

$$D_C = \bar{A}\bar{C}D + \bar{A}C\bar{D}$$

$$D_D = \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D} \text{ (LSB)}$$



∴ this system has the property of self correct.



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