Shift Register:-

A register capable of shifting its binary information either to the right or to the left. The logical configration of a shift register consists of a chain of F.Fs. Connected to the input of the next f.f. All F.F receive a common clock pulse which causes the shift from one stage to the next. There are two ways to shift data into a register serial (shifting data at a time in a serial begining with LSB) or Parallel (shifting all the data bit simultaneously). This leads to the construction of four baisc register types:-

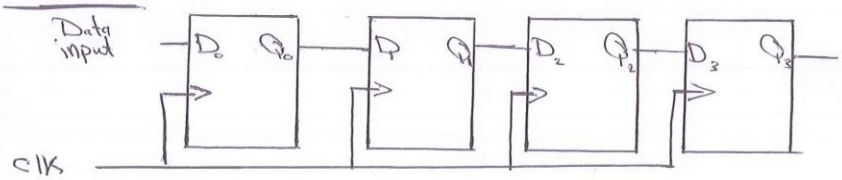
1- Serial In- Serial out (SI-SO).
2- Serial In- Parallel out (SI-PO).
3- parallel In- Serial out (PI-So).
4- parallel In- Parallel out (PI-PO).

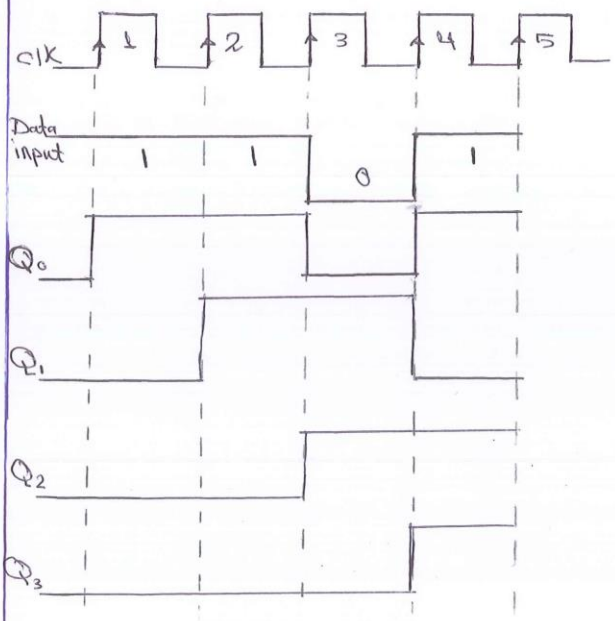
1- Serial In - Serial Out (SI-SO) shift register:-

The (SI-SO) shift register accepts data serially that is, one bit at a time on a single line. It produced the stored information on its output also in serial form.

Example:- Draw the waveform to shift the number 1101 into the shift register. Assume the register is initially cleared (all 0's)?

Solution:-

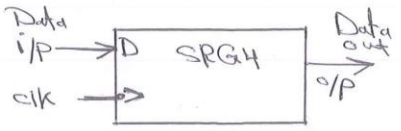


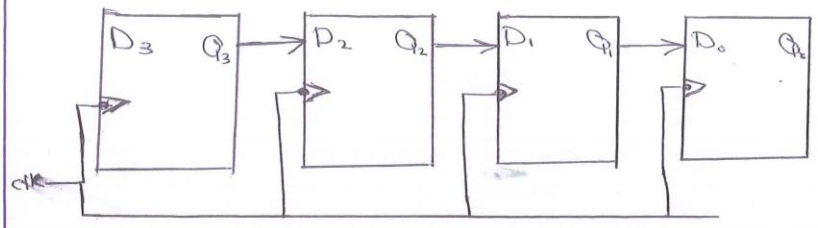


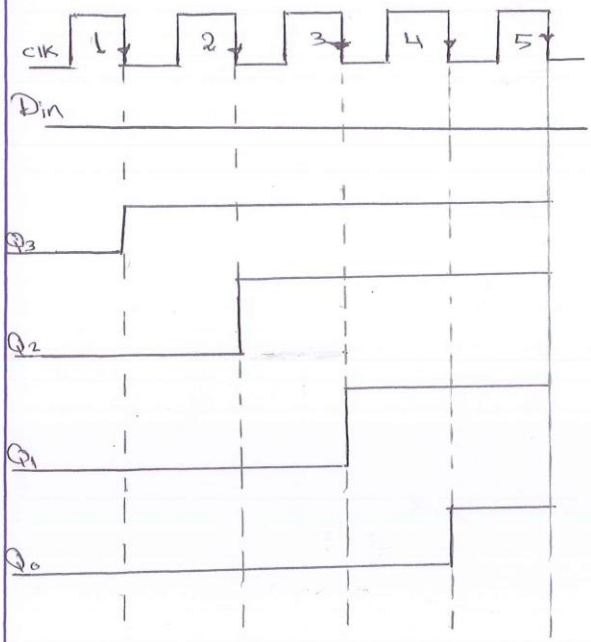
CLK	Q_0	Q_1	Q_2	Q_3
initially	0	0	0	0
1-CLK ↑	1	0	0	0
2-CLK ↑	1	1	0	0
3-CLK ↑	0	1	1	0
4-CLK ↑	1	0	1	1

Example:- Draw the waveform to shift the number 1111 in to the shift register. Assume the register is initially cleared?

Solution:-







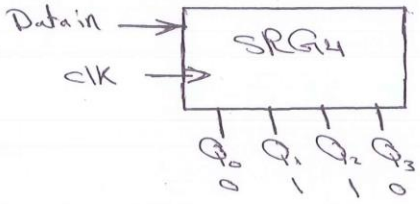
clk	Q_3	Q_2	Q_1	Q_0
initially	0	0	0	0
1-cp↓	1	0	0	0
2-cp↓	1	1	0	0
3-cp↓	1	1	1	0
4-cp↓	1	1	1	1

2- Serial Input-parallel out (SIPO) shift register:-

A (SI-PO) shift register is similar to the (SISO) shift register in that it shifts data into internal storage elements and shifts data out at the serial-out, data out, pin. It is different in that it makes all the internal stages available as outputs. Therefore, a serial-in/parallel out shift register converts data from serial format to parallel format.

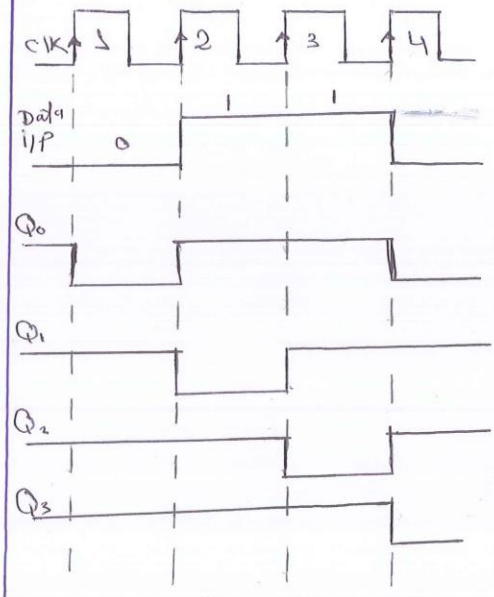
Example:- Show the states of the 4 bit shift register (SRG4) for the data input and clock pulse waforms in figure below. The register initially contains all 1's?

Solution:-



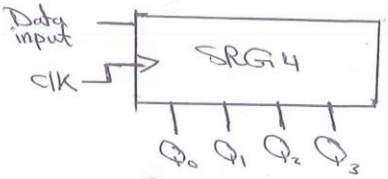
Data input = 0110_0

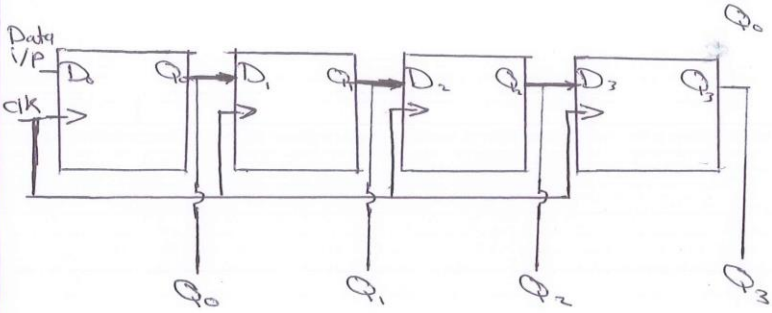
clk	Q_0	Q_1	Q_2	Q_3
initially	1	1	1	1
1-cp↑	0	1	1	1
2-cp↑	1	0	1	1
3-cp↑	1	1	0	1
4-cp↑	0	1	1	0

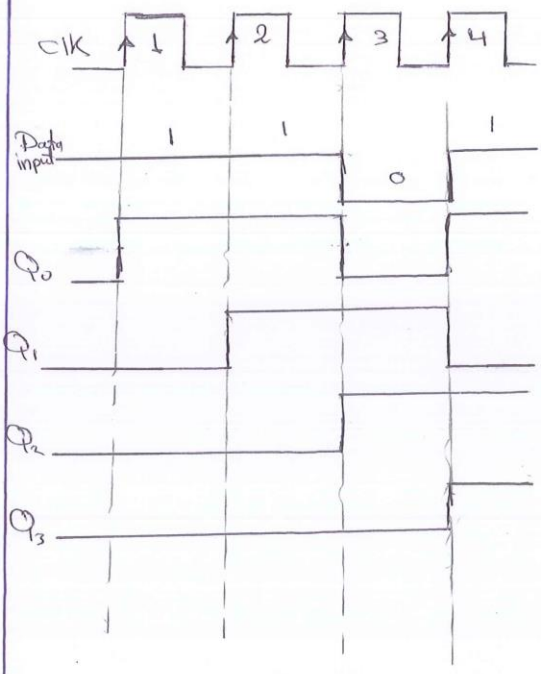


Example:- The bit sequence 1101 is serially entered into a 4-bit parallel out shift register (SRG4) that is initially cleared. what are the Q outputs after three clock pulse.

Solution:-







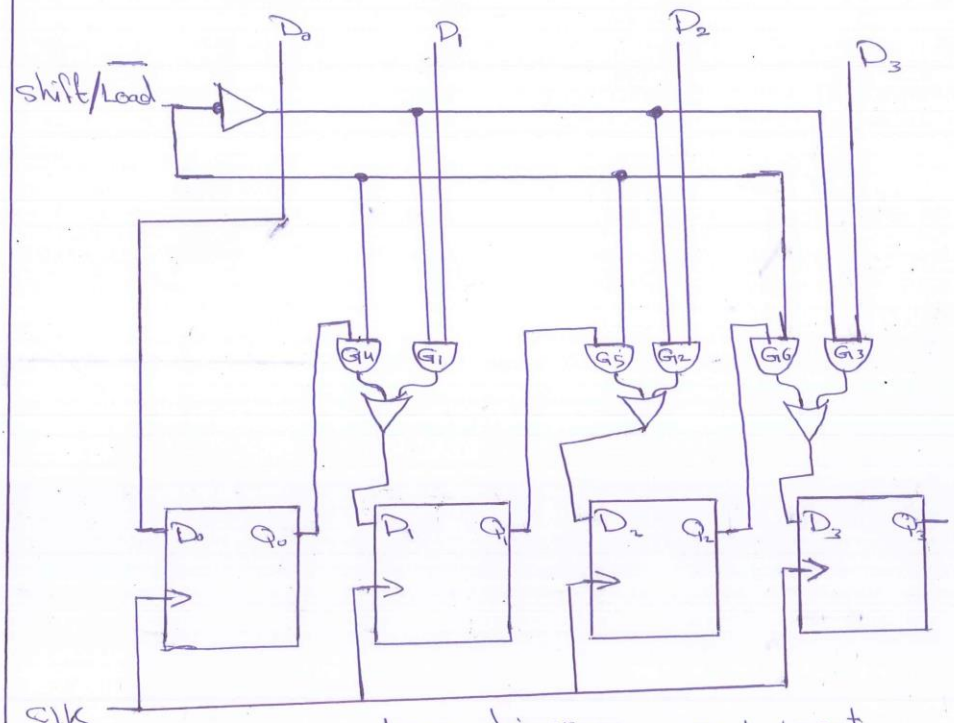
CLK	Q_0	Q_1	Q_2	Q_3
initially	0	0	0	0
1-cp ↑	1	0	0	0
2-cp ↑	1	1	0	0
→ 3-cp ↑	0	1	1	0
4-cp ↑	1	0	1	1

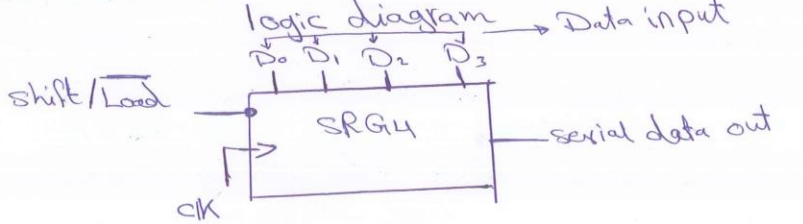
The Q output (0110) after three clock pulses.

3-Parallel In-Serial out (PISO) shift registers:-

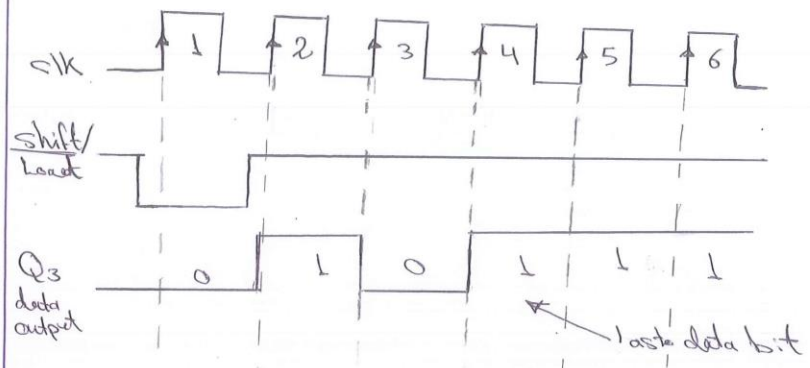
For a register with parallel data input, the bits are entered simultaneously into their respective stages on parallel lines rather than on a bit-by-bit basis on one line as with serial data inputs. The serial outputs is the same as the (SISO) shift register, once the data are completely stored in the register.

The 4-bit (PISO) shift register and a typical logic symbol are shown below:-





Solutions:-



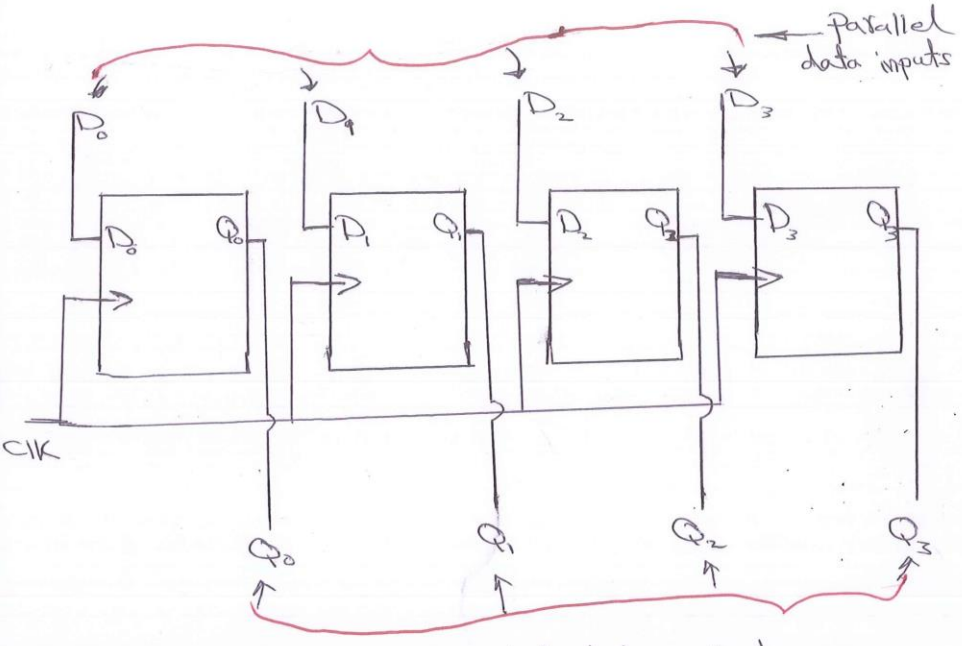
- At clock (1) the parallel data (D_0, D_1, D_2, D_3) = 1 0 1 0 are loaded into the register making Q_3 a (0).
- At clock (2) the (1) is shifted from Q_2 into Q_3.
- At clock (3) the (0) is shifted from Q_2 into Q_3.
- At clock (4) the last data bit (1) is shifted onto Q_3.
- At clock (5) all data bits have been shifted out only 1s remain in the register.

CLK	Q_0	Q_1	Q_2	Q_3
CLK_1	1	0	1	0
CLK_2	0	1	0	1
CLK_3	0	0	1	0
CLK_4	0	0	0	1

4- Parallel In- Parallel out (PIPO) shift registers:-

In this register, immediately following the simultaneous entry of all data bits, the bits appear on the parallel output.

A 4 bit parallel In-Parallel out shift register is as follows:-



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