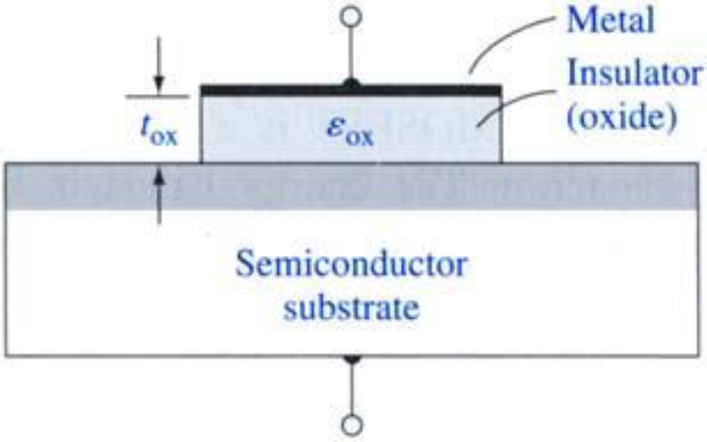
Metal-Oxide-Semiconductor

The two-terminal MOS structure

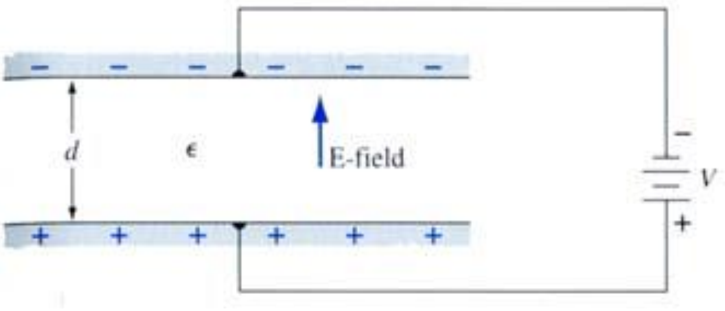
- The MOS capacitor perform is the basic core of the MOS transistor
- The metal is a high-conductivity polycrystalline silicon
- The parameter tox is the oxide thickness
- The oxide permittivity is ε_{ox}
- The Si-SiO$_2$ interface is also referred to as the surface of the semiconductor



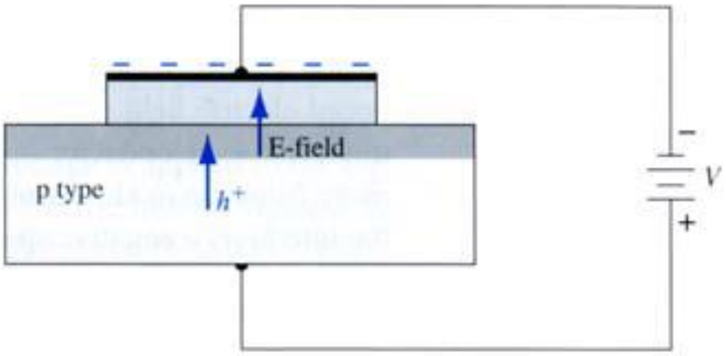
Energy-Band Diagrams p-type substrate: accumulation region

- In a simple parallel-plate capacitor we have

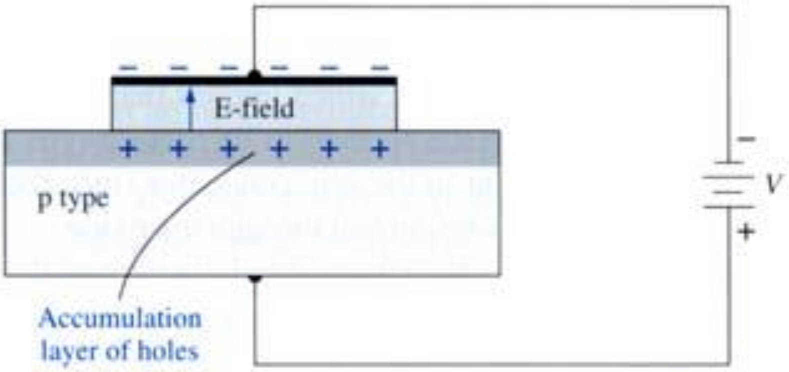
$$C' = \frac{\varepsilon}{d} \qquad Q' = C'V \qquad E = \frac{V}{d}$$

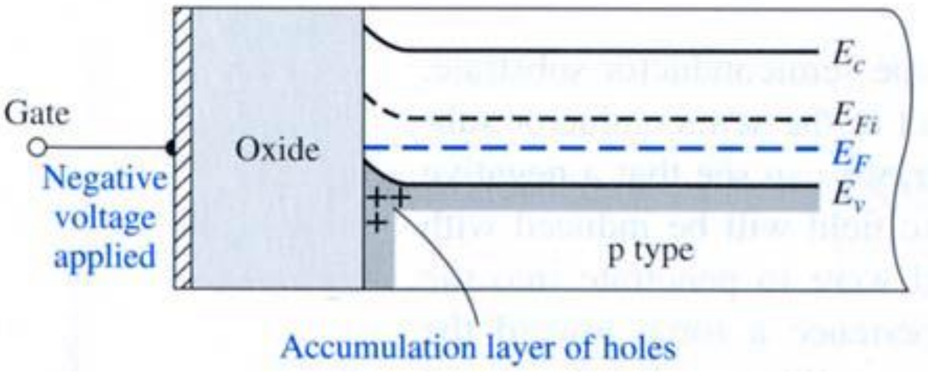


- ❑ In a MOS capacitor with a p-type substrate, when the metal is negatively charged, the semiconductor is positively charged
- ❑ The positive charge in the semiconductor is made of holes
- ❑ Holes accumulates at the Si-SiO_2 interface



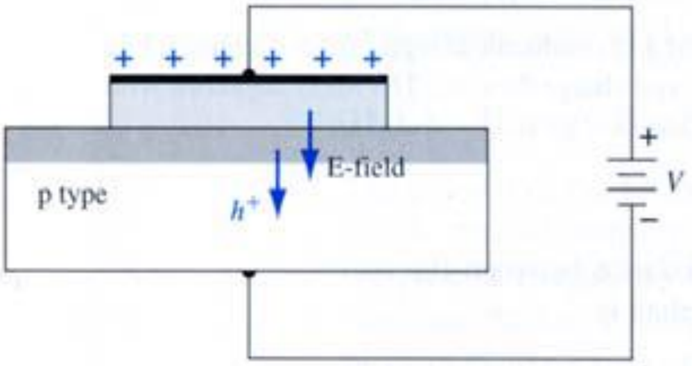
- ❑ In a MOS capacitor with a p-type substrate, when the holes accumulate at the Si-SiO2 interface, the bands bend
- ❑ The valence-band edge is closer to the Fermi level at the Si-SiO_2 interface than in the bulk material
- ❑ The band bending expresses the accumulation of holes

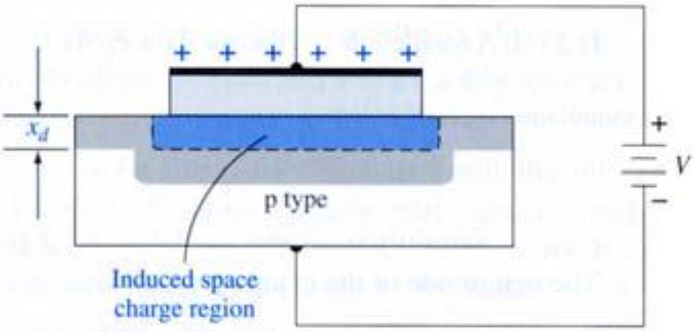




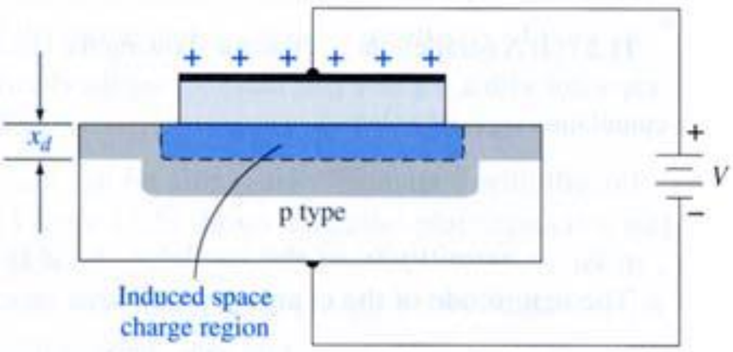
Energy band diagrams p-type substrate: depletion region

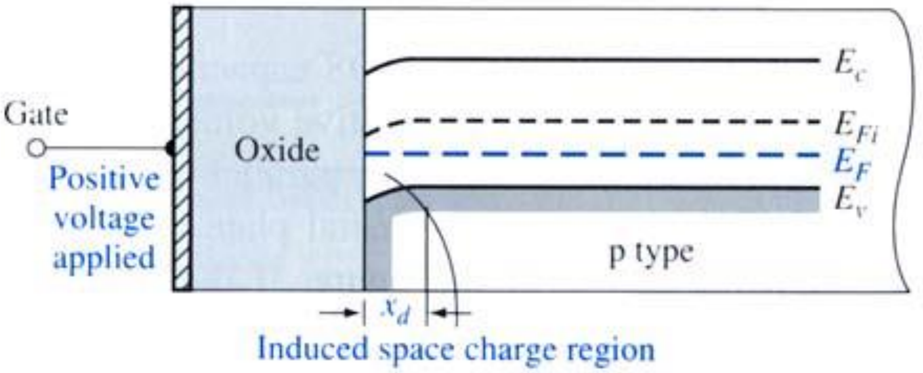
- ❑ If a positive charge exists on the top metal plate, a negative charge is induced in the semiconductor
- ❑ Holes are pushed away from the electric field and a negative space-charge region is created
- ❑ The **depletion region** extends from the silicon-oxide interface up to x_d (depletion region width)
- ❑ It is responsible for the negative charge in the bottom plate of the MOS capacitor





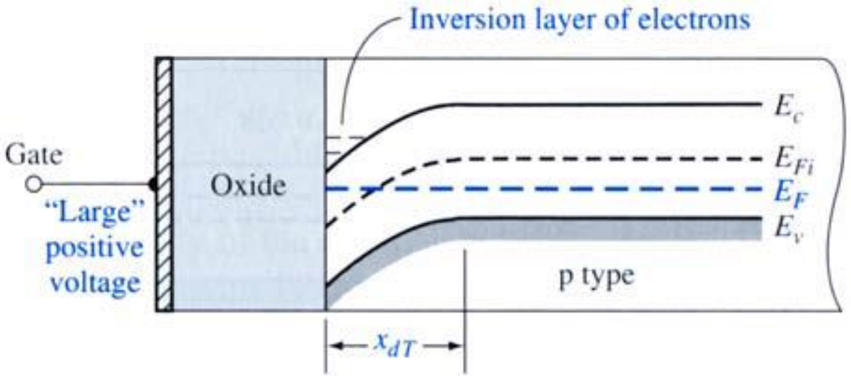
- In a MOS capacitor with a p-type substrate, when the holes are pushed away from the Si-SiO_2 interface, the bands bend
- The conduction band and the intrinsic Fermi level move closer to the Fermi level
- The band bending expresses the repulsion of holes



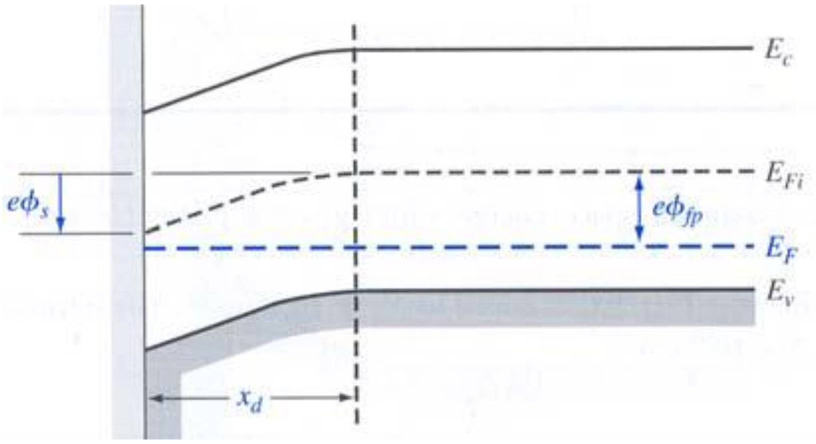


Energy band diagrams p-type substrate: inversion region

- Increasing the positive voltage applied to the top metal gate increases the electric field as well
- A larger negative charge in the semiconductor implies a larger induced depletion region and more band bending
- When the intrinsic Fermi level at the Si-SiO2 interface moves below the Fermi level, the conduction band is closer to the Fermi level than the valence band is
- At the surface, the semiconductor becomes n-type
- An inversion layer of electrons is created



Depletion Layer Thickness



- ☐ In the bulk semiconductor the difference between E_{Fi} and E_F may be related as

$$\phi_{fp} = \frac{E_{Fi} - E_F}{e} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

- ☐ The difference between E_{Fi} at the surface and E_{Fi} in the bulk semiconductor is the *surface potential*

$$\phi_s = \phi_{(xd)} - \phi_{(0)} = \frac{E_{Fi(xd)} - E_{Fi(0)}}{e}$$

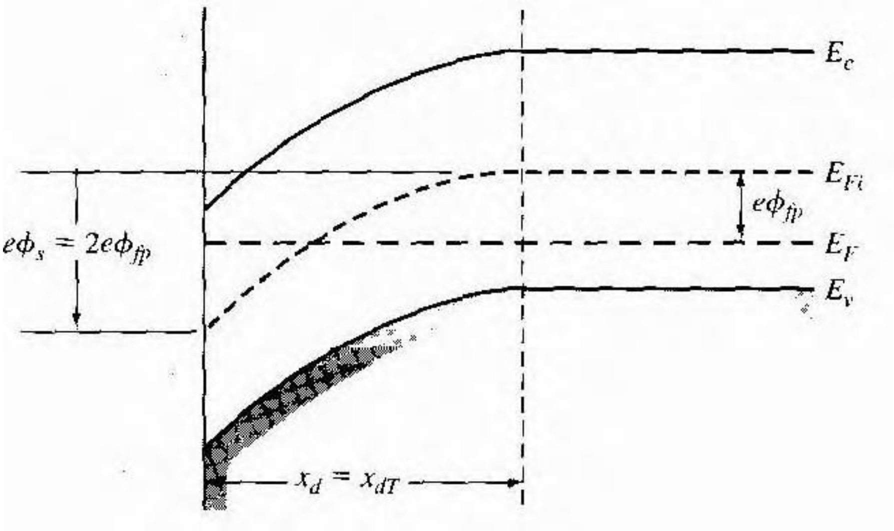
- ☐ Under the abrupt depletion layer approximation, we may relate the depletion layer thickness to the surface potential

$$x_d = \left(\frac{2\varepsilon_s \phi_s}{eN_a}\right)^{1/2}$$

- ☐ When $\Phi_s = 2\Phi_{fp}$ the electron concentration at the surface is the same as the hole concentration in the bulk material
- ☐ The space charge has a maximum Width

$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{fp}}{eN_a} \right)^{1/2}$$

- ☐ This is the threshold inversion point



Example

To determine maximum space charge width. Consider p-type Si doped with $N_a = 10^{16}$ cm^{-3}. Let T = 300 K so that $n_i = 1.5 \times 10^{10}$ cm^{-3}.

Solution

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i} \right) = 0.0259 \ln\left(\frac{10^{16}}{1.5 \times 10^{10}} \right) = 0.347V$$

$$x_{dT} = \left(\frac{4\varepsilon_s \phi_{fp}}{eN_a} \right)^{1/2} = \left(\frac{4(11.7)(8.85 \times 10^{-14})(0.347)}{(1.602 \times 10^{-19})(10^{16})} \right)^{1/2}$$

$$x_{dT} = 0.3 \times 10^{-4} cm = 0.3 \mu m$$

TEST YOUR UNDERSTANDING

E11.1 (*a*) Consider as oxide-to-p-type silicon junction at **7** = 300 K. The impurity doping concentration in the silicon is N, = 3 × 10^{16} cm^{-3}. Calculate the maximum space-charge width in the silicon. (*b*) Repeat part *(a)* for an impurity concentration of $N_a = 10^{15}$ cm^{-3}. [Ans. (*a*) 0.180 μm, (*b*) 0.863 μm]

E11.Z Consider an oxide-to-n-type silicon junction at T = 300 K. The impurity doping concentration in the silicon is N_d = 8 x 10^{15} cm^{-3}. Calculate the maximum space-charge width in the silicon. (Ans. 0.33 μm)

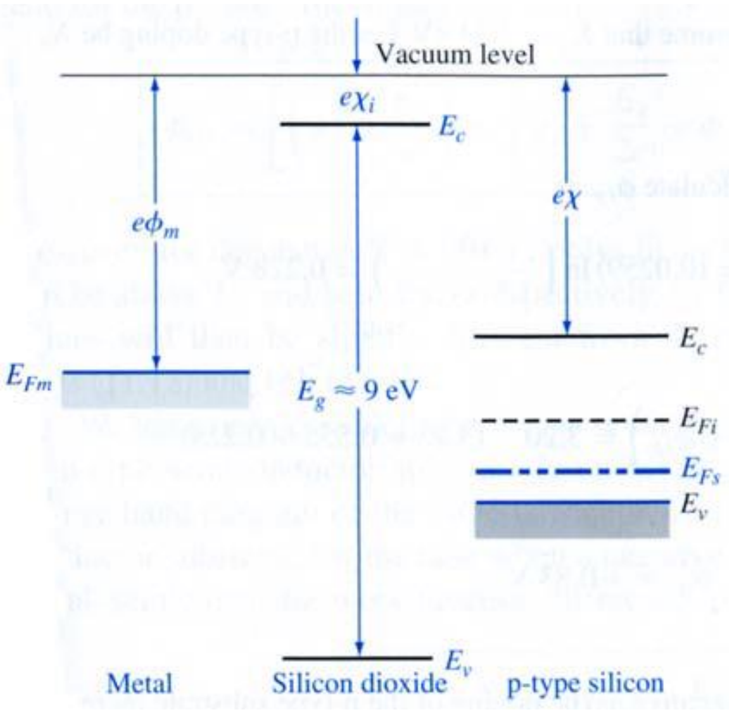
Work function differences

- ☐ χ_i is the insulator electron affinity
- ☐ In the case of silicon dioxide χ_i = 0.9 V
- ☐ We define

$$\phi_m' = \phi_m - \chi_i$$

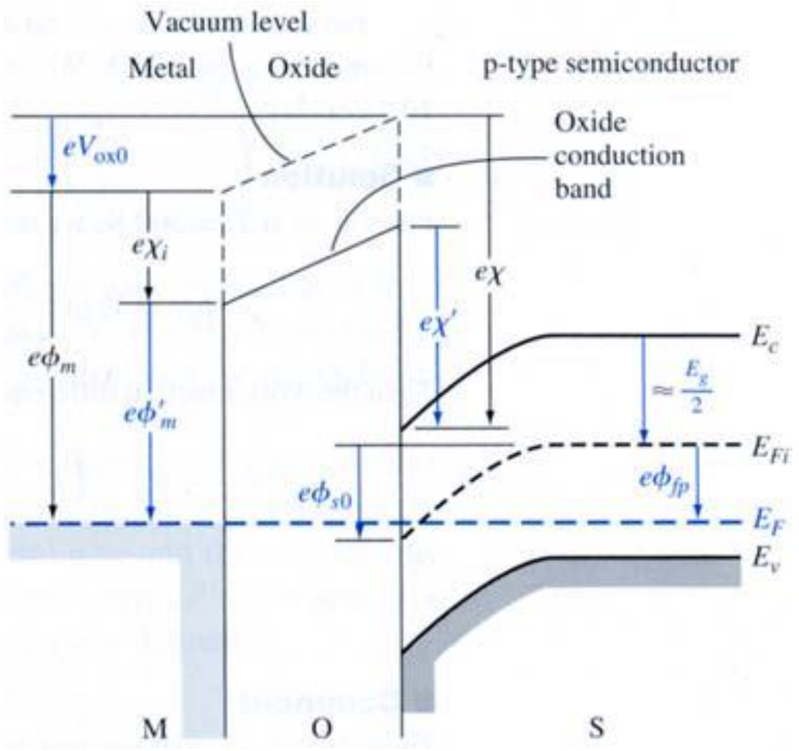
$$\chi' = \chi - \chi_i$$

as the modified metal work function and the modified electron affinity



- ☐ The energy-band diagram through the MOS structure in thermal equilibrium after contact.

- The voltage V_{ox0} is the potential drop across the oxide for zero applied gate voltage and is not necessarily zero because of the difference between Φ_m *and X*.
- Potential Φ_{s0} *is the* surface potential for this case.
- We can define a potential Φ_{ms} as which is known as the metal-semiconductor work function difference



The equation can be rewritten as

$$\phi_{ms} = \left[\phi_m - \left(\chi + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$

- The structure experiences a voltage drop

$$\phi_{ms} = \left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$

$$e\phi'_m + eV_{ox0} = e\chi' + \left(\frac{E_g}{2}\right) - e\phi_{s0} + e\phi_{fp}$$

$$V_{ox0} + \phi_{s0} = -\left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$

$$V_{ox0} + \phi_{s0} = -\phi_{ms}$$

Example

Calculate the metal-semiconductor work function difference Φ_{ms} for a given MOS system. For an aluminum-silicon dioxide junction $\Phi'_m = 3.20$ V and for a silicon-silicon dioxide junction, $\chi' = 3.25$ V. We may assume that E_g = I. I eV Let the p-type doping be $N_a = 10^{14}$ cm^{-3}.

Solution

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = 0.0259\ln\left(\frac{10^{14}}{1.5\times10^{10}}\right) = 0.228V$$

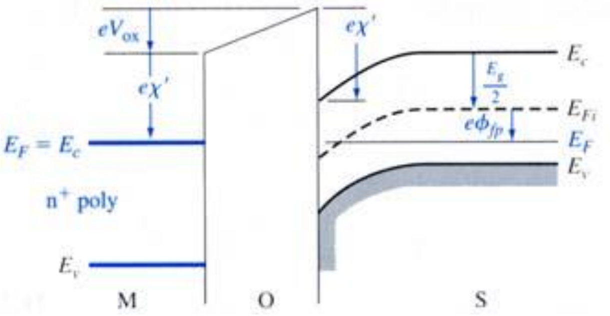
$$\phi_{ms} = \left[\phi_m^{'} - \left(\chi^{'} + \frac{E_g}{2e} + \phi_{fp}\right)\right] = 3.2 - (3.25 + 0.555 + 0.228 = -0.83V$$

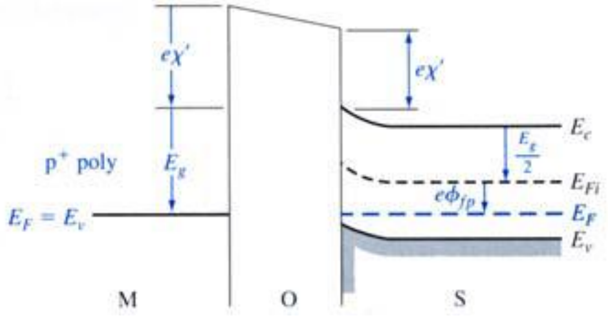
Work function differences: Polysilicon case

- ☐ Degenerately doped polysilicon is often used as the gate

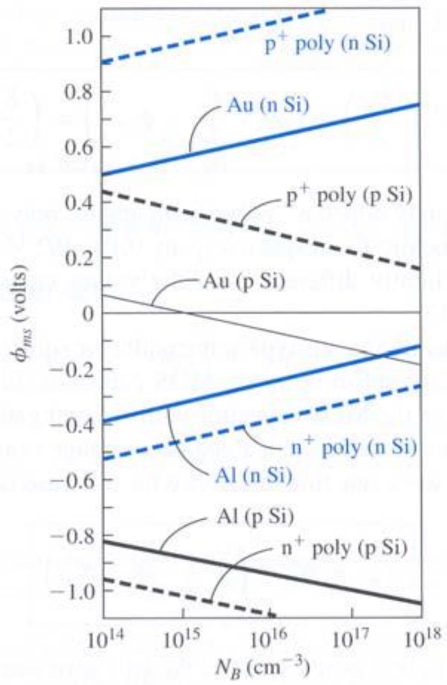
$$\phi_{ms} = \left[\chi^{'} - \left(\chi^{'} + \frac{E_g}{2e} + \phi_{fp}\right)\right] = -\left(\frac{E_g}{2e} + \phi_{fp}\right)$$

- ☐ For the p+ polysilicon gate, we have $\Phi_m \approx \chi + E_g / e$





$$\phi_{ms} = \left[\left(\chi^{'} + \frac{E_g}{e}\right) - \left(\chi^{'} + \frac{E_g}{2e} + \phi_{fp}\right)\right] = \left(\frac{E_g}{2e} - \phi_{fp}\right)$$



TEST YOUR UNDERSTANDING

E11.3 The silicon impurity doping concentration in an aluminum–silicon dioxide–silicon MOS structure is $N_a = 3 \times 10^{16}$ cm^{-3}. Using the parameters in Example 11.2, determine the metal-semiconductor work function difference ϕ_{ms}. (Ans. $\phi_{ms} = -0.981$ V)

E11.4 Consider an n$^+$ polysilicon gate in an MOS structure with a p-type silicon substrate. The doping concentration of the silicon is $N_a = 3 \times 10^{16}$ cm^{-3}. Using Equation (11.12), find the value of ϕ_{ms}. (Ans. $\phi_{ms} = -0.931$ V)

E11.5 Repeat E11.4 for a p$^+$ polysilicon gate using Equation (11.13). (Ans. $\phi_{ms} = +0.119$ V)