DECODERS & ENCODERS

Object: To study the function of decoder and encoder circuits

Theory:

(A) *Decoder:*

A decoder is a combinational circuit that converts coded information, such as binary, into a recognizable form, such as decimal. Fig. (7-1) shows a 2-to-4 line decoder circuit. The two inputs are decoded into four outputs, each output representing one of the minterms of the 2-input variables. The two inverters provide the complement of the input, each one of the minterms. However, a 2-to-4 line decoder can be used for decoding any 2-bit code to provide four outputs, one of each element at the code.

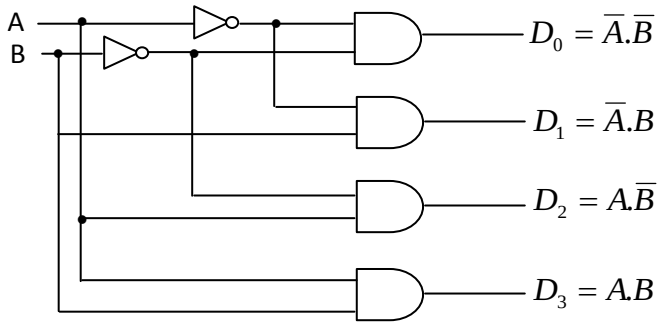

Fig.(7-1) A logic circuit of 2-to-4 line decoder

The operation of the decoder may be further classified from it's input-output relationships, listed in table(7-1) observe that one output variable are mutually exclusive because only one output can be equal to 1 at one time.

INPUTS		OUTPUTS			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table (7-1) Truth table of a 2-to-4 line decoder

(B) *Encoder:*

The encoder is also a combinational logic circuit; it converts information, such as a decimal number or an alphabetic character, into some coded form such as binary or BCD.

The octal-to-binary encoder consists of eight inputs, one for each of the eight digits, and three outputs that generate the corresponding binary number. It is constructed with OR gates whose inputs can be determined from the truth table given in table(7-2). The lower-order output bit Z is 1 if the input octal digit is odd. Output X is 1 for octal digits 4, 5, 6 or 7. Note that D_0 is not connected to any OR gate, the binary inputs are all 0's.

The encoder in Fig.(7-2) assumes that only one input line can be equal to 1 at any time; otherwise the circuit has no meaning.

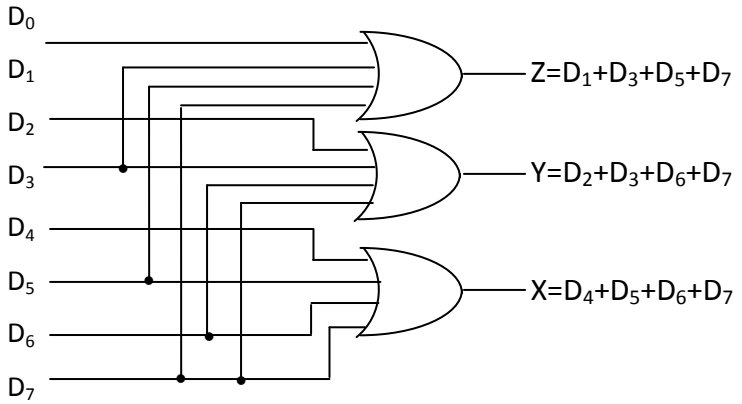

Fig. (7-2) Logic diagram of Octal-to-binary encoder

Note that the circuit has eight inputs and could have 2^8=256 possible input combinations. Only eight of these combinations have any meaning. The other inputs combinations are don't care conditions. The operation of the encoder listed in table (7-2).

INPUTS								OUTPUTS		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Table (7-2) Truth table of an Octal-to-binary encoder

Procedure:

(A) *Decoder:*

1. Connect the circuit as shown in Fig.(7-1) using NAND gates only. Check it's truth table.
2. Design a BCD-to-Decimal decoder using NAND gates only.

(B) *Encoder:*

1. Connect the circuit as shown in Fig.(7-2) using NAND gates only. Check its truth table.

Discussion:

1. Design a 3-bit binary decoder (3-to-8 decoder), then construct this circuit using NOR gates only.
2. Design a BCD-to-seven segment decoder (7447 IC).