Mustansiriyah University
College of Engineering
Electrical Engineering Dept.
Second Class

Date: 24/4/2019
Time: 90 Minutes
Examiners: Lect. Dr. Ammar Ghalib
Lect. Noor Safaa
Asst. Lect. Basma Nazar

Digital Techniques II

Q1) Design a synchronous counter by means of T flip-flops and any necessary logic gates to count the sequence (0, 1, 2, 4, 5, 6). Assuming the counter has the property of self-starting, self-stopping and self-correcting to the initial state.

(5 marks)

Q2) For a special X-Y Flip Flop of the following characteristic table; X and Y are inputs and Q_n is the present state.

X	Y	Q_n	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

1. Derive the excitation table of this flip flop.
2. Design a synchronous counter which counts the repeated sequence: {0, 1, 3}; using X-Y flip flops.

(5 marks)

Q3) Answer **(A)** or **(B)**:

(A) Design a BCD ripple counter using J-K flip-flops of asynchronous clear and pre-set and any necessary logic gates.

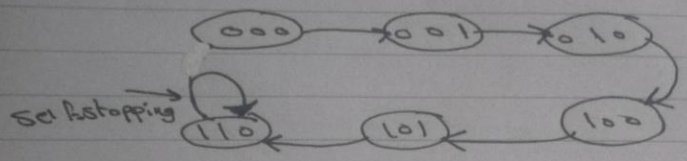
(B) Explain briefly the main differences between synchronous and asynchronous counters. Give an example for each type.

(5 marks)

حلول اسئلة امتحان نهاية السنة مادة التقنيات الرقمية
المرحلة الثانية.

Q1:- 0 → 1 → 2 → 4 → 5 → 6

self correction xxx → 000
self stopping 110 → 110



State diagram

Present state			Next state					
C_n	B_n	A_n	C_{n+1}	B_{n+1}	A_{n+1}	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	1	0	0	1	1	0
0	1	1	0 0 0			0	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	0	0	0	0
1	1	1	1 1 1			1	1	1

self correction → X X X

State table

A \ CB	$\bar{C}\bar{B}$	$\bar{C}B$	CB	$C\bar{B}$
$\bar{A}$	0	1	0	0
A	0	0	1	0

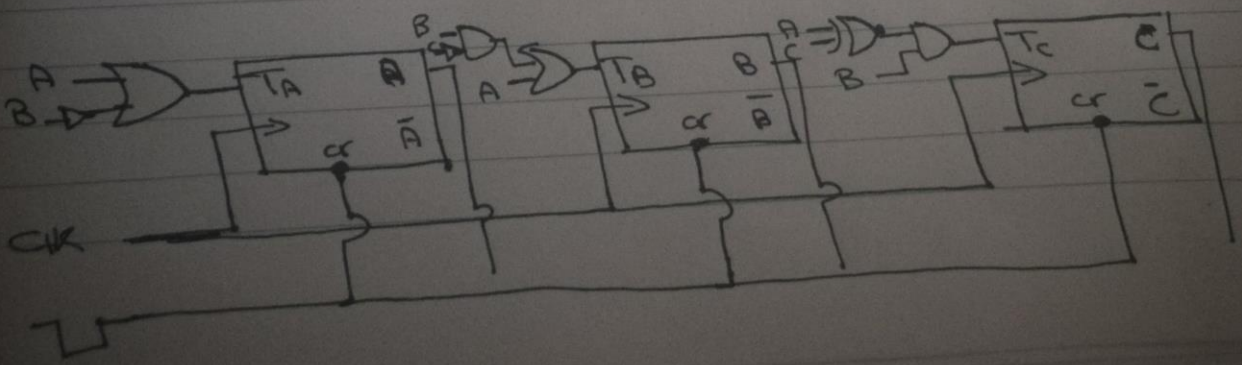
A \ CB	$\bar{C}\bar{B}$	$\bar{C}B$	CB	$C\bar{B}$
$\bar{A}$	0	1	0	0
A	1	1	1	1

A \ CB	$\bar{C}\bar{B}$	$\bar{C}B$	CB	$C\bar{B}$
$\bar{A}$	1	0	0	1
A	1	1	1	1

$T_C = (\bar{A}B\bar{C} + ABC)$
$= B(A \odot C)$

$T_B = (B\bar{C} + A)$

$T_A = (A + \bar{B})$

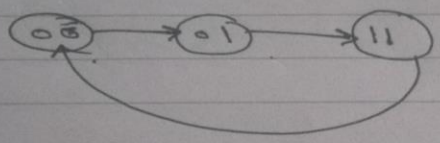


Q2:-

Q_n	Q_{n+1}	X	Y
0	0	1	X
0	1	0	X
1	0	X	1
1	1	X	0

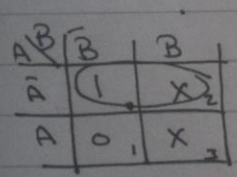
① Excitation table

②

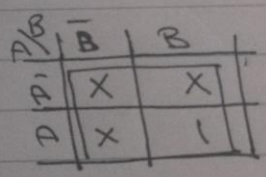


State diagram

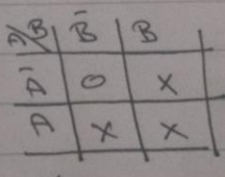
Present state B_n	A_n	Next state B_{n+1}	A_{n+1}	X_B	Y_B	X_A	Y_A
0	0	0	1	1	X	0	X
0	1	1	1	0	X	X	0
1	0	X	X	X	X	X	X
1	1	0	0	X	1	X	1



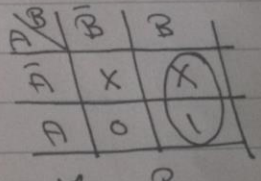
$X_B = \bar{A}$



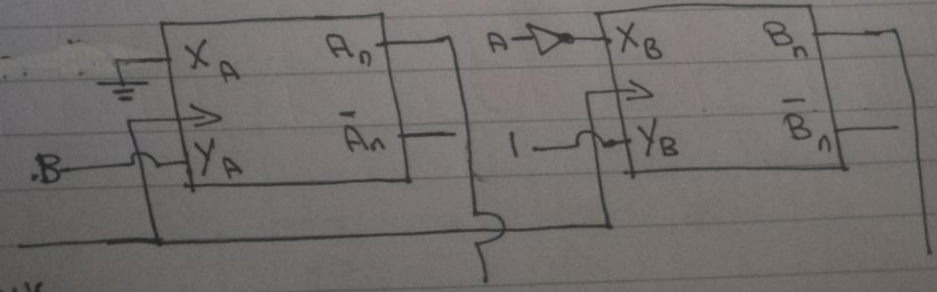
$Y_B = 1$



$X_A = 0$

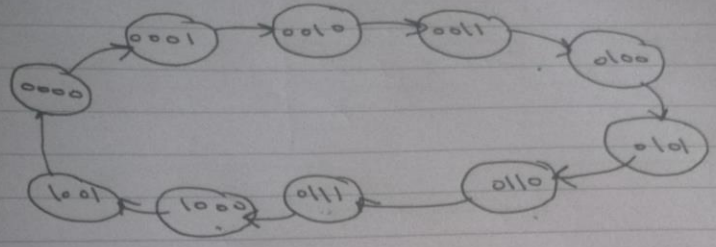


$Y_A = B$



CIK

Q3A:- BCD ripple counter (mod 10)



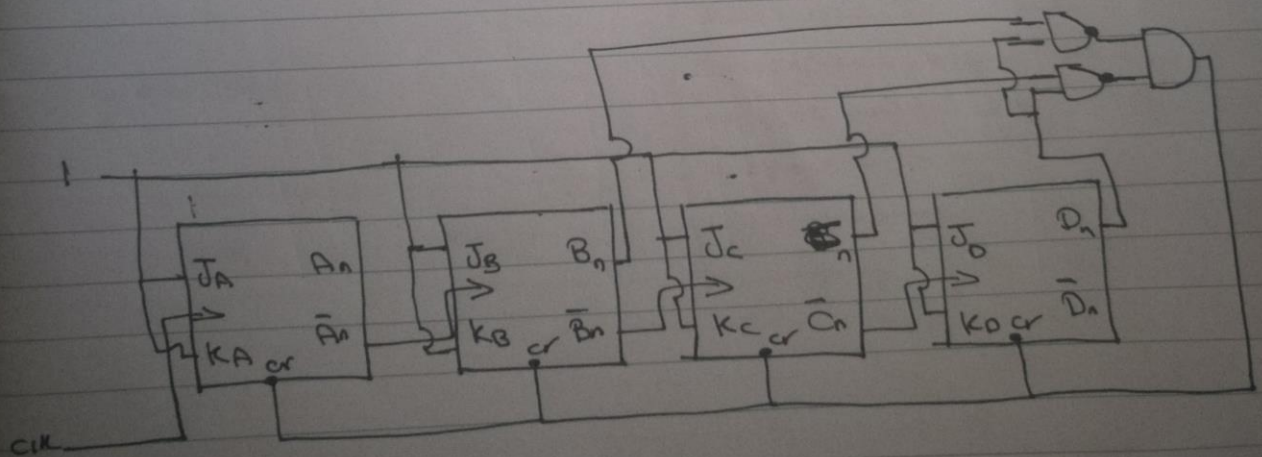
10, 11, 12, 13, 14, 15

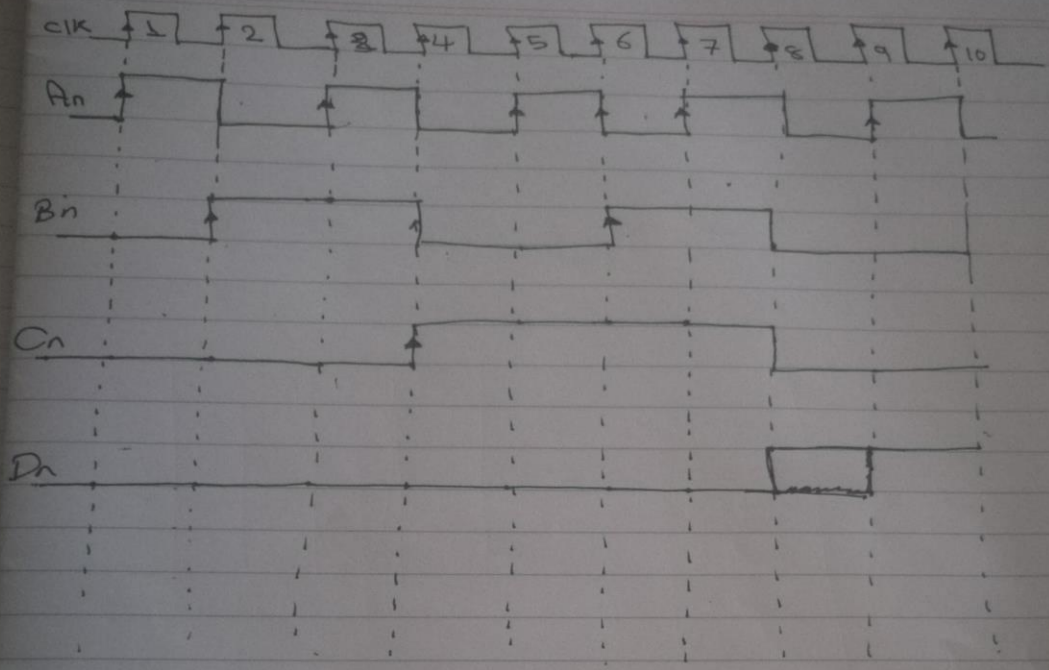
$B_n A_n$ \ $D_n C_n$	$\bar{D}\bar{C}$	$\bar{D}C$	DC	$D\bar{C}$
$\bar{B}\bar{A}$	0	4	12	8
$\bar{B}A$	1	5	13	9
$B\bar{A}$	3	7	15	11
$B\bar{A}$	2	6	14	10

$F = D_C + DB$

$F = \overline{D_C} \cdot \overline{DB}$

CLK	States D_n C_n B_n A_n
initially	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1





Q3B/

Synch. Counter	Asynch. Counter
The clock input is connected to all of the Flip-Flops; so that they are clocked simultaneously	The First Flip-Flop is clocked by external clock pulse and then each successive Flip-Flops is clocked by the output of the preceding Flip-Flop.