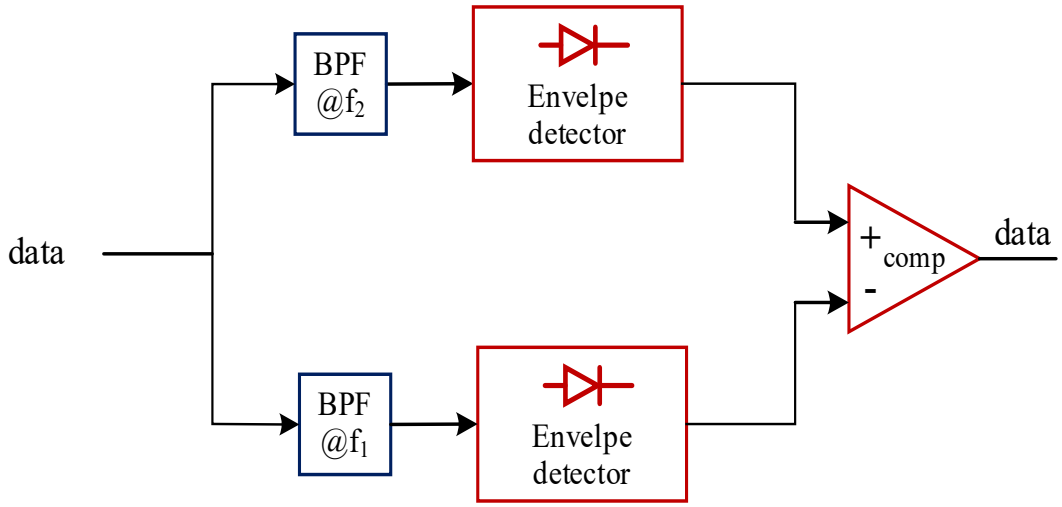
Demodulator of FSK:

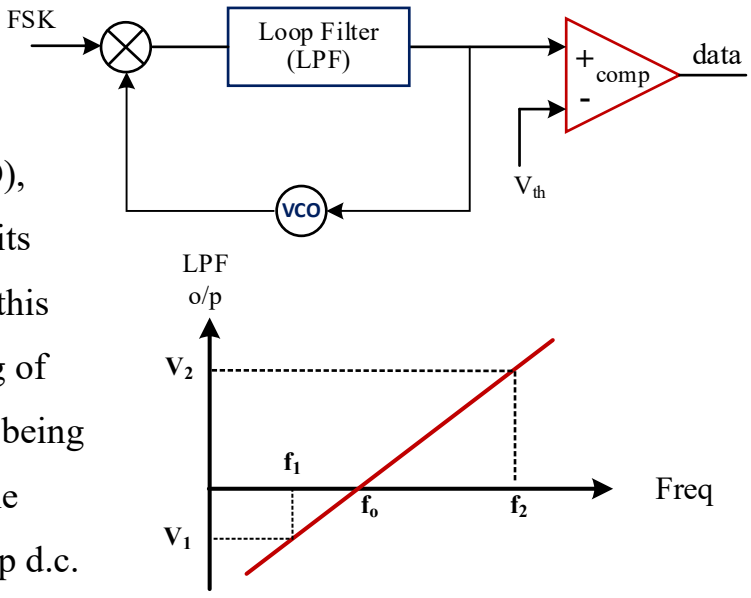
1) **Noncoherent detector:** (no need for carrier recovery)

   Two BPF are used, one tuned at f_2 and the other at f_1. A high output will appear at the corresponding arm for logic "0" or logic "1".



2) **Coherent PLL (Phase Locked Loop) detector:**

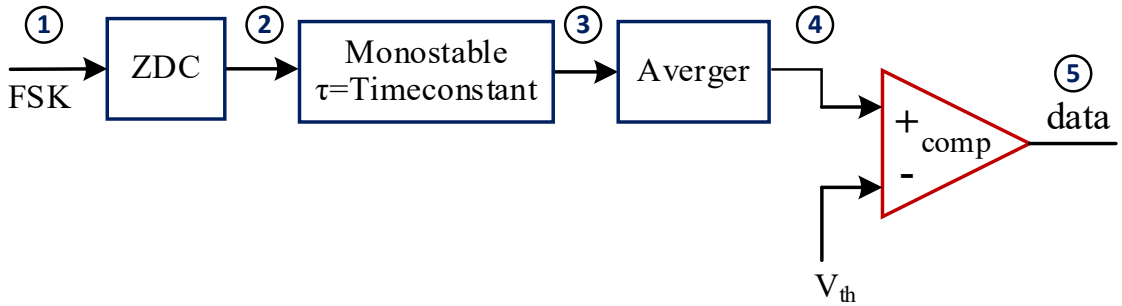
A phase locked loop (PLL) consists of a phase detector (PD), loop filter (LPF) and a VCO at its feedback. The characteristic of this PLL against frequency charging of the input is shown besides of $\mathbf{f_o}$ being the free running frequency of the VCO (its frequency o/p when i/p d.c. is zero).



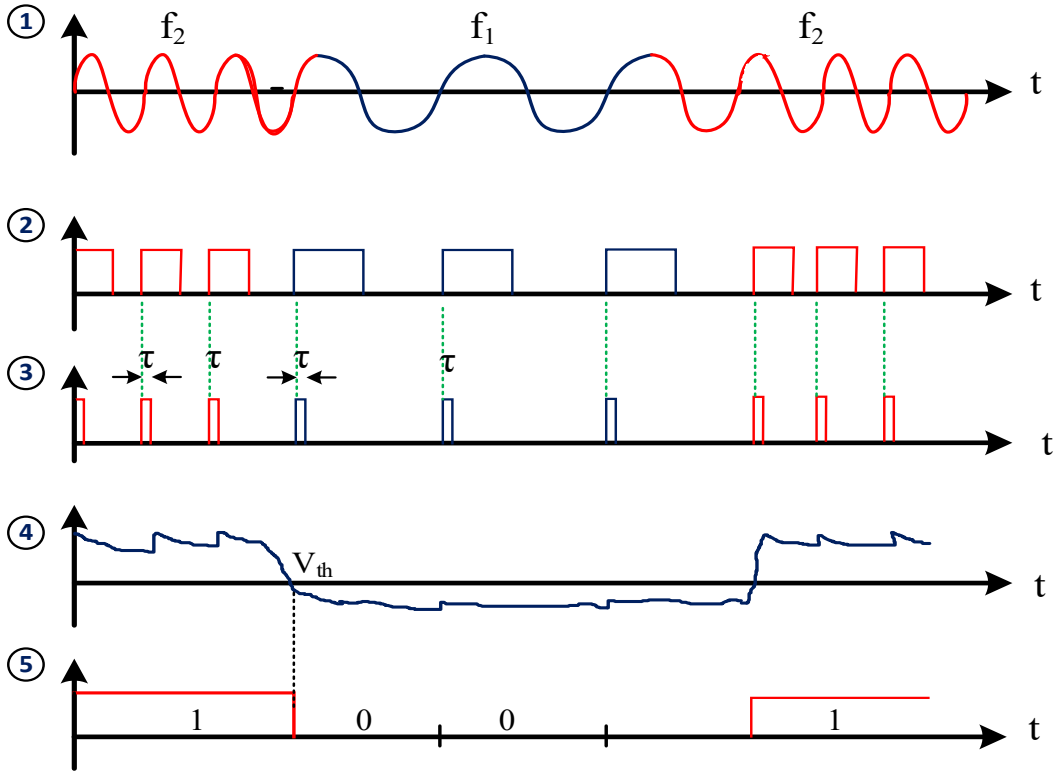
$$V_{th} = \frac{V_1 + V_2}{2} \quad \text{... (6-27)}$$

A threshold comparator with $V_{th} = \frac{V_1+V_2}{2}$ is adjusted to give the received data using a threshold comparator.

3) Zero Crossing Frequency Discriminator:



The zero crossing detector (ZDC) changes sinewave into rectangular waves with frequencies f_1 and f_2.



The positive going edge monostable gives fixed time constant τ chosen such that $\tau \leq (\frac{1}{f_2})$. The average value of the monostable output is high level for frequency f_2 and is low level for frequency f_1. A threshold comparator with a threshold V_{th} chosen midway between the high & low value will give data output.

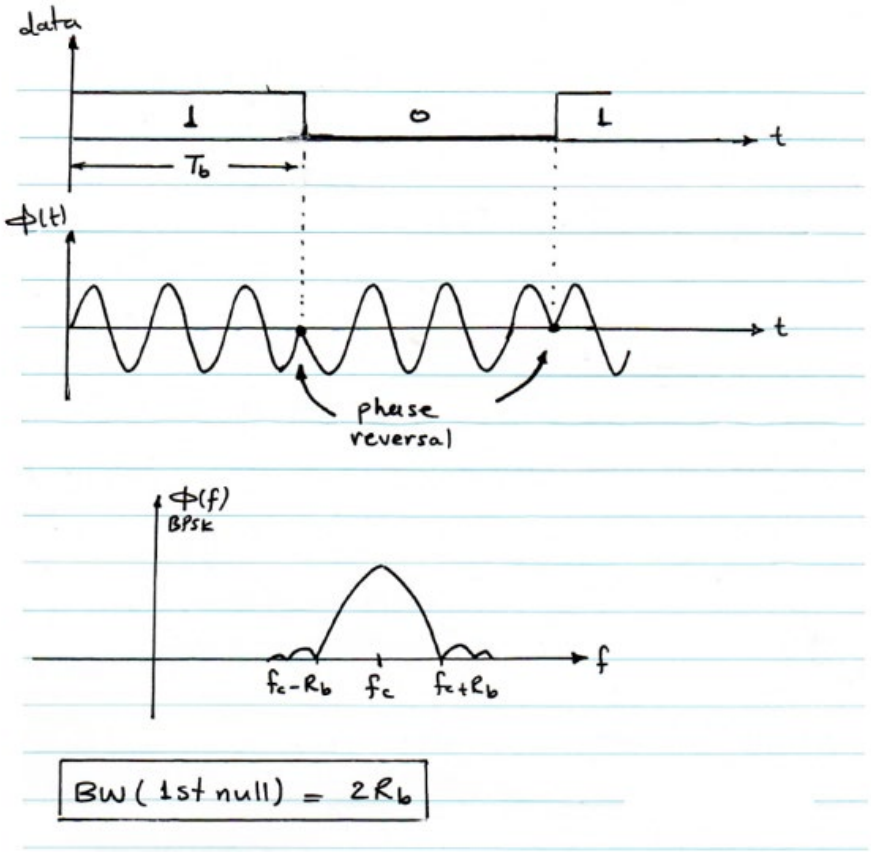
3- Phase Shift Keying (PSK):

$$\emptyset_0(t) = A\cos\omega_c t$$

$$\emptyset_1(t) = A\cos(\omega_c t + \pi) = -A\cos\omega_c t$$

Over bit duration T_b ... (6-25)

When there is only two phases to describe data values. The modulation is called Binary Phase Shift Keying (BPSK).



Ex 6-14

Find the minimum bandwidth for a BPSK signal transmitting at 2000 bps. The transmission mode is half-duplex.

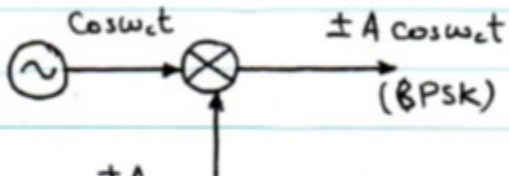
Solution:

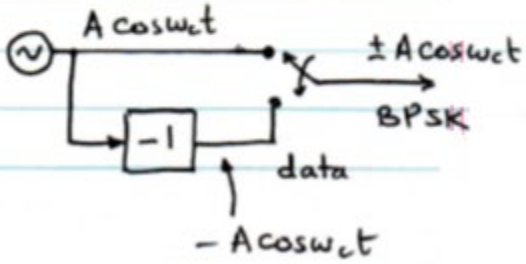
$BW = 2R_b = 2*2000 = 4kHz$

Modulator Design:

A balanced modulator (mixer) is used to generate PSK, at high data rate.

For lower data rate, simple analogue switch controlled by a data can be used to generate PSK.

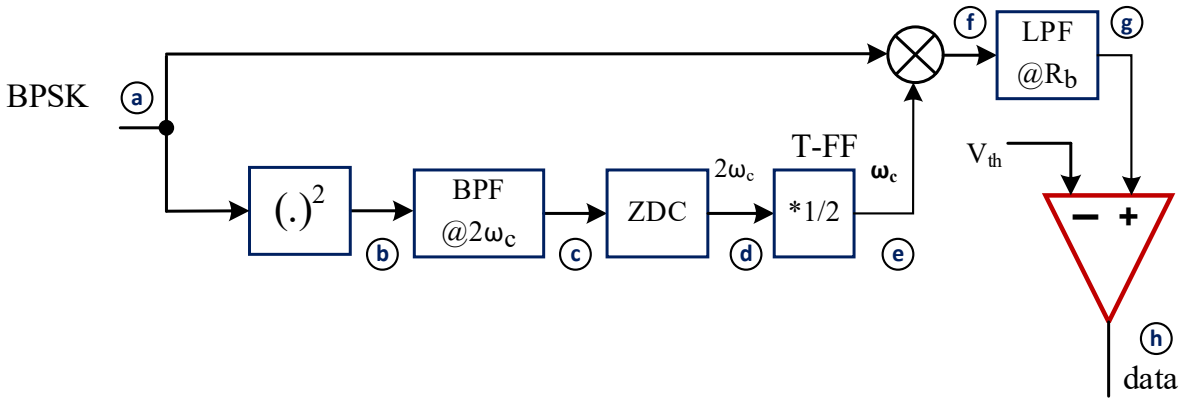


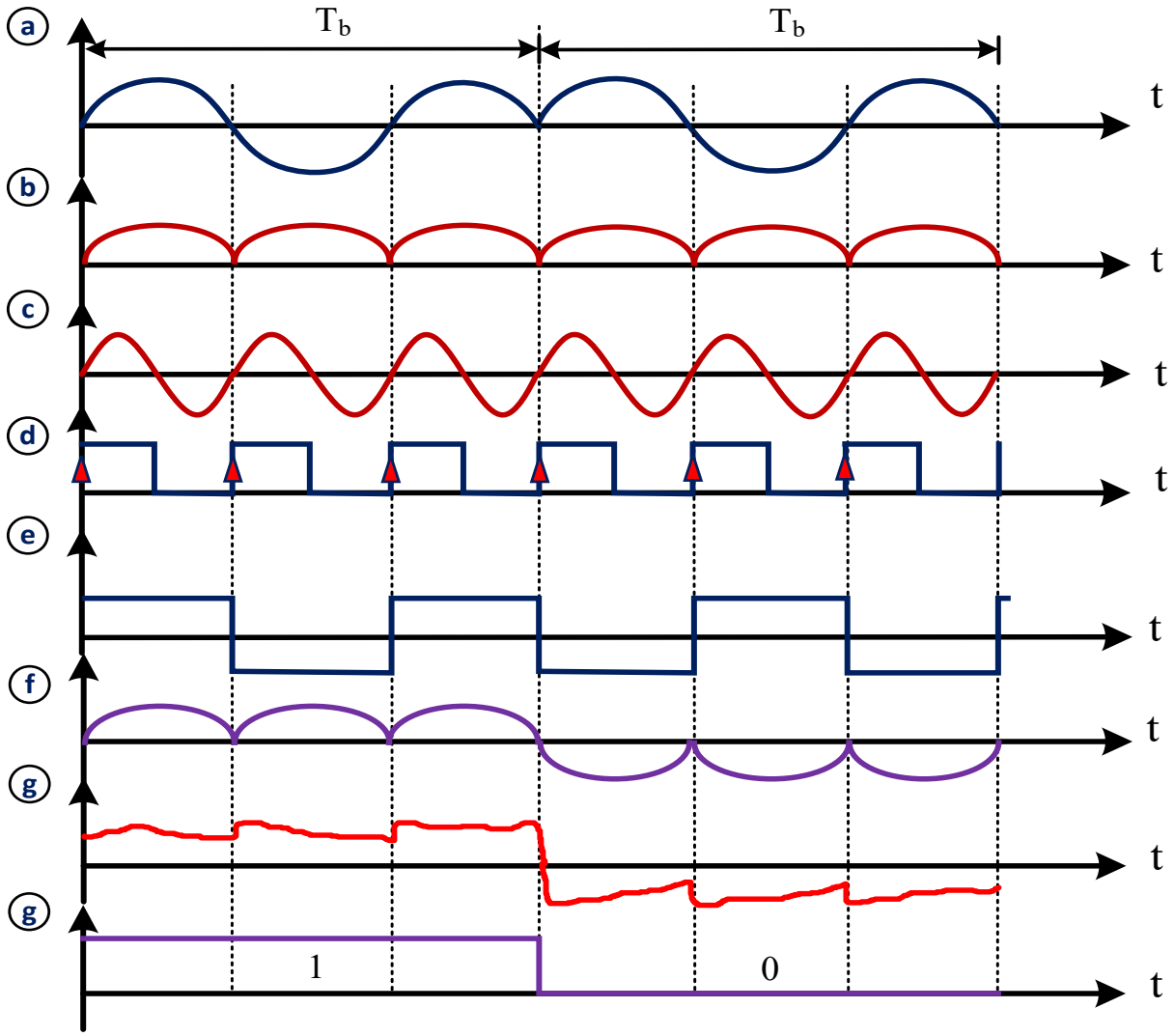


PSK demodulator:

Since information is the phase of the carrier, then only coherent PSK is possible, i.e. coherent carrier phase must be generated at the receiver.

Carrier Recovery (Squaring Loop):

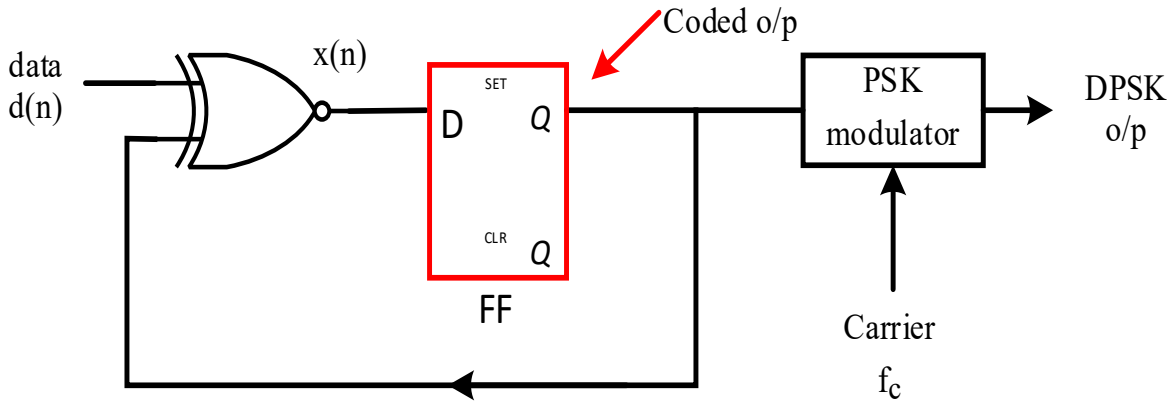




The $\pm A\cos\omega_c t$ PSK modulation is first canceled using squarer to give $\frac{A^2}{2}(1+\cos\omega_c t)$, the double carrier frequency is filtered using BPF tuned at $2\omega_c$, then T-FF is used to generate carrier at ω_c with correct phase.

Differential PSK (DPSK)

There is possibility in PSK detection that the receiver will receive "0" as "1" or "1" as "0" (i.e. data complement) due to he initial phase of the carrier (phase ambiguity). To solve this problem, a technique called differential PSK (DPSK) is used. The encoder of the DPSK is shown below:



The coded output x(n) is obtained from transmitted data using:

$x(n) = \overline{d\,(n)}\;\overline{\quad\quad} + x\;\overline{(n\;\;-1)}$, where $+\equiv Ex-OR$

i.e exclusive-NORing previous output code with present data. x(n) then transmitted using conventional PSK modulator with 0° and 180° phase shift for logic "0" and logic "1". The extra requirement for DPSK noncoherent detection is the analogue delay liner T_b and then multiply with itself, LPF then a threshold comparator.

Ex 6-15

Find the output coded sequence and the carrier phase for data input : $d(n) = 11011001\ldots$

Solution:

For any random choice of the initial content of the D-F/F the DPSK coder will work successfully.
For example if initial state of D-FF is logic "1" then:
$X(0) = 1$, & $X(1) = \overline{d(1) + x(0)} = \overline{1+1} = 1$ and so on.

n	0	1	2	3	4	5	6	7	8	...
data d(n)		1	1	0	1	1	0	0	1	...
x(n)	1	1	1	0	0	0	1	0	0	...
phase (rad)	π	π	π	0	0	0	π	0	0	...

DPSK decoder:

- The decoder of DPSK does not need correct phase of the carrier and hence DPSK is sometimes called noncoherent PSK (DPSK ≡ noncoherent PSK)