Mustansiriyah University

College of Engineering

Electrical Engineering Dept.

Fundamentals of Logic Circuits Laboratory

First Year

Object: To study the operation of magnitude comparator.

Theory:

An A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitudes. The outcome of comparison is specified by three binary variables that indicate whether A>B, A=B, or A< B. the EX-OR gate is a basic comparator because its output is 1 if it's two input bits are not equal and is 0 if the inputs are equal. Fig (5.1) shows the EX-OR as a 2-bit comparator.

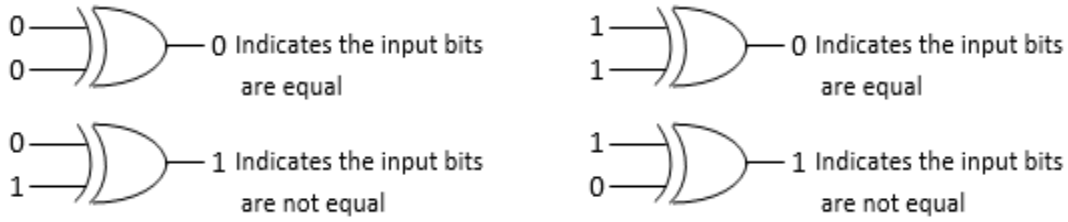


Fig. 5.1. Basic Comparator Operation

The circuit for comparing two n-bit numbers has 2^{2n} entries in the truth table, and becomes too cumbersome even with n=3. Table (5.1) shows how to compare two numbers having 1-bit.

Table 5.1: Truth Table of 1-bit Comparator

INPUTS		OUTPUTS		
A	B	Z1 A=B	Z2 A>B	Z3 B<A
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

From table (5-1), using minterms, we see that:

$$Z1 = A.B + \bar{A}.\bar{B}$$
$$Z2 = A.\bar{B} \qquad \text{..... (5.1)}$$
$$Z3 = \bar{A}.B$$

From these expressions, we may obtain the digital circuit by using AND, OR, and NOT gates. The result is shown in Fig (5.2).

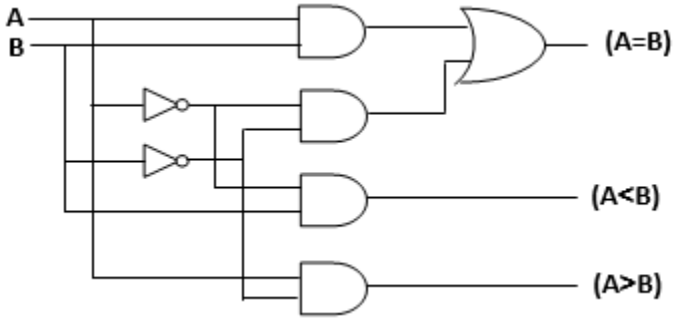


Fig. 5.2. Logic Circuit of 1-bit Comparator

The general algorithm for designing a n-bit comparator has the following steps (i.e. 4-bit).

a) Write the coefficients of the number as follows:

A= A_3 A_2 A_1 A_0

B= B_3 B_2 B_1 B_0

Where each subscribed letter represents one of the digits in the number.

b) For A=B (A_3=B_3, A_2=B_2, A_1=B_1, A_0=B_0), this can logically be expressed with an equivalence function:

$$X_i = A_i.B_i + \overline{A_i}.\overline{B_i} \qquad i = 0, 1, 2, 3, \ldots, n \qquad \text{..... (5.2)}$$

where X_i=1 only if the pair of bits in position *i* are equal.

In order to determine whether A>B or A<B, compare the relative magnitudes of pair of significant digits starting from the MSB position. If the two digits are equal, we compare the next lower significant pair of digits. This comparison continues until a pair of unequal digits is reached. If the corresponding digit of A is 1 and of B is 0, we conclude that A>B. if the corresponding digit of A is 0 and that of B is 1, we have A<B.

The sequential comparison can be expressed logically by:

$$(A>B)=A_3\overline{B_3} + X_3A_2\overline{B_2} + X_3X_2A_1\overline{B_1} + X_3X_2X_1A_0\overline{B_0}$$

$$(A<B)=\overline{A_3}B_3 + X_3\overline{A_2}B_2 + X_3X_2\overline{A_1}B_1 + X_3X_2X_1\overline{A_0}B_0 \quad \ldots\ldots (5.3)$$

From these expressions, we may obtain the digital comparator circuit as shown in Fig. (5.3).

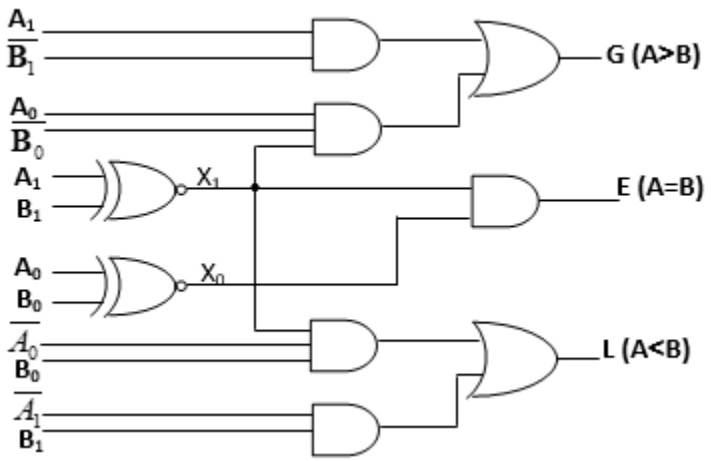


Fig. 5.3. Logic Circuit of 2-bit Comparator

Procedure:

1- Implement 1-bit comparator using logic.ly then verify the truth table.

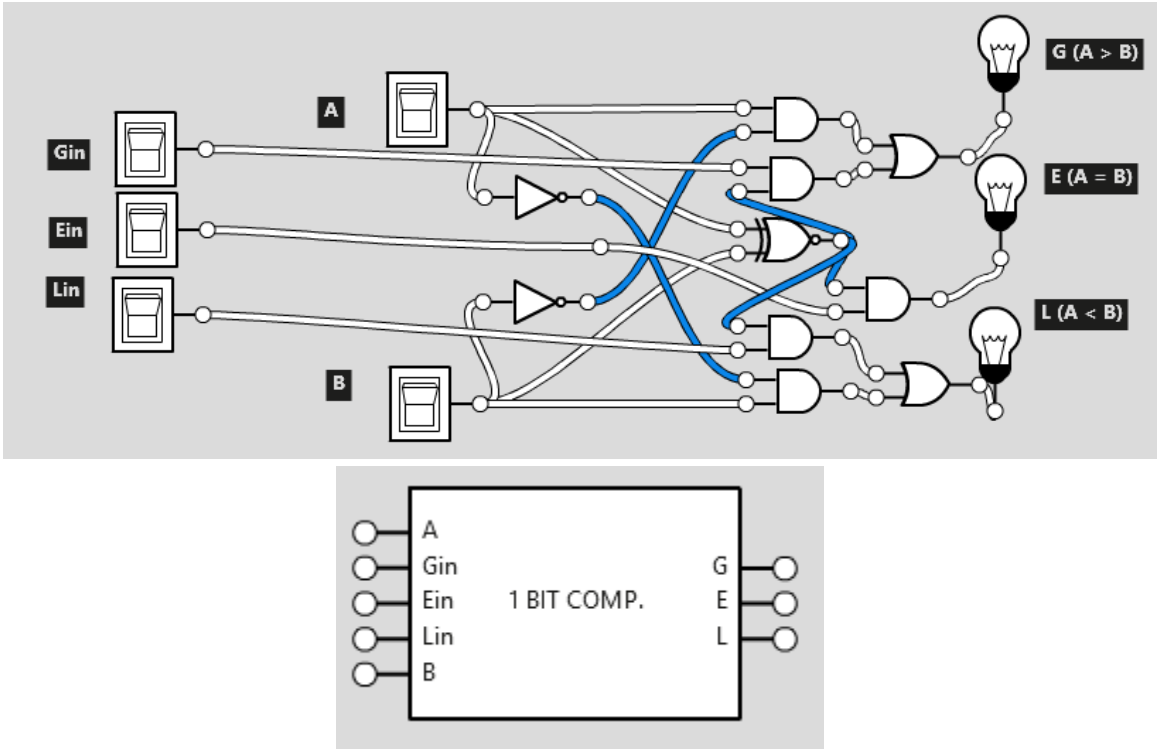
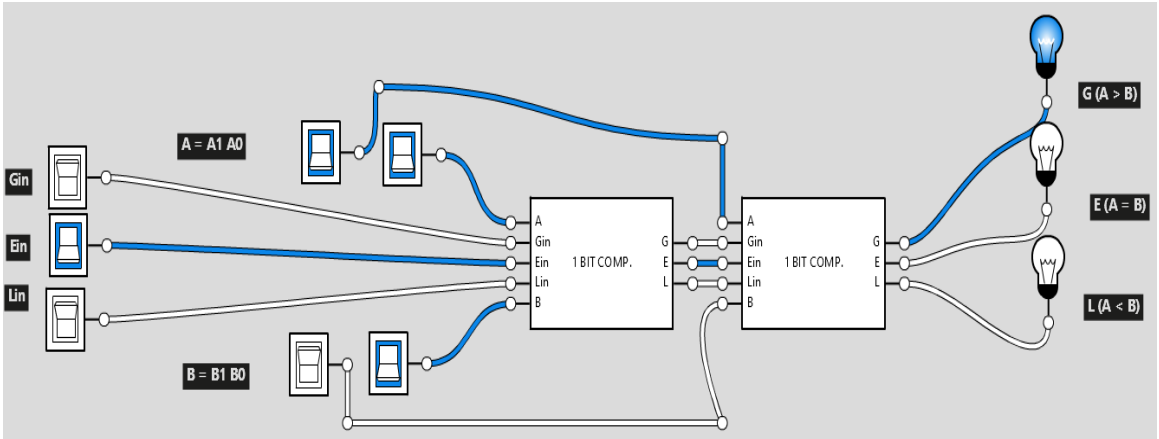


Fig. 5.4. Implementation of 1-bit Comparator using Logic.ly

2- Implement 2-bit comparator using logic.ly then verify the truth table.



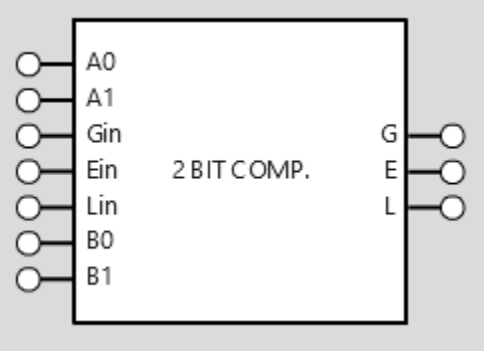
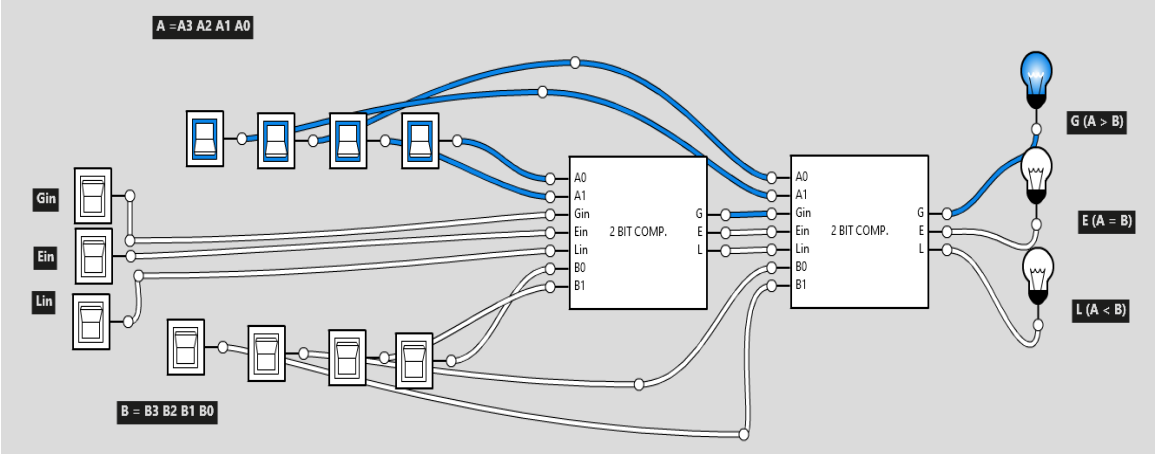


Fig. 5.5. Implementation of 2-bit Comparator using Logic.ly

3- Implement 4-bit comparator then verify the truth table. (***This circuit represents 7485 IC***).



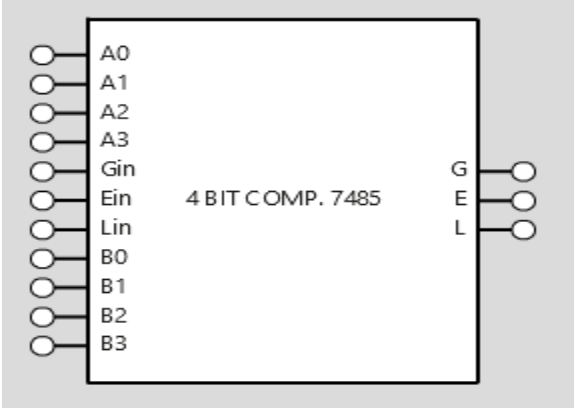
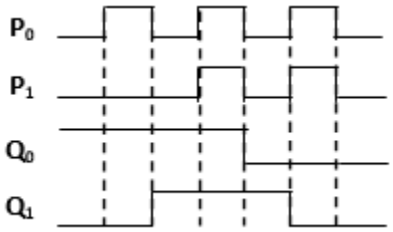
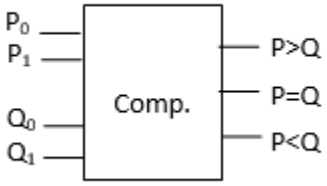


Fig. 5.6. Implementation of 4-bit Comparator using Logic.ly

Discussion:

1. If the waveforms shown in Fig. below are applied to the comparator, find the output waveforms.





2. Given the logic symbol for the *7485 IC* (4-bit comparator). Use it to compare two binary numbers of 12 bit.

3. For each of the following set of binary numbers, determine the logic states at each output of *7485 IC* (4-bit comparator).

   $P = P_3\ P_2\ P_1\ P_0 = 1001$

   $Q = Q_3\ Q_2\ Q_1\ Q_0 = 1101$

4. Design a logic circuit to compare 1-bit binary numbers, using NAND gates only.