Mustansiriyah University

College of Engineering

Electrical Engineering Dept.

Fundamentals of Logic Circuits Laboratory

First Year

Object: To design and implement logic circuit for basic arithmetic operations.

Theory:

An important part of the central processor of any computer is the arithmetic unit in which binary addition, subtraction, division and multiplication are carried out.

Subtraction however can be performed by adding complemented numbers. Multiplication can also be performed by repeated addition. Division can be also achieved by repeated subtraction. This means that the adder is the centre piece of the arithmetic unit. There are two types of the addition:

1. Half - Adder (HA):

It is a device that adds two bits of binary data. In other words, the half adder performs the operations:

$$0 + 0 = 0$$
$$0 + 1 = 1 \qquad \ldots\ldots. (4.1)$$
$$1 + 0 = 1$$
$$1 + 1 = 0, \quad \text{Carry} = 1$$

The last operation is, of course, 1+1=0, which is 0 with a carry 1 to the next bit position. Equation (4.1) may be expressed n the form of a truth table as shown in table (4.1). From the truth table we see that

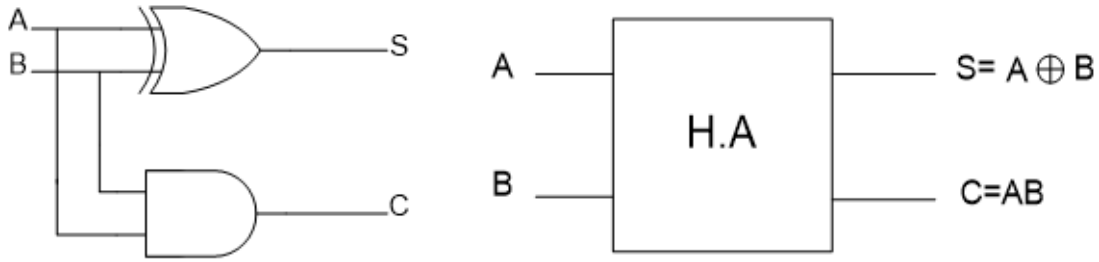
$$S = A\bar{B} + \bar{A}B \qquad \ldots\ldots. (4.2)$$
$$= A \oplus \text{B}$$

and $C = A.B \qquad \ldots\ldots. (4.3)$

Table 4.1: Truth Table of Half Adder (HA)

Input		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

So, the HA adds only two bits at a time, so that it cannot be used to add two bits and a carry bit from a previous step. The circuit diagram and symbol of the HA is given in Fig (5.1).



(a) (b)

Fig. 4.1. Half Adder (HA): (a) Circuit diagram; (b) Block symbol

2. Full - Adder (FA):

A half adder is not very useful on its own, and a third input is often required for carries. Adding numbers that have two bits or more requires a full adder (FA) which is capable of the previous order. The symbol of full-adder is shown in Fig. (4.2).

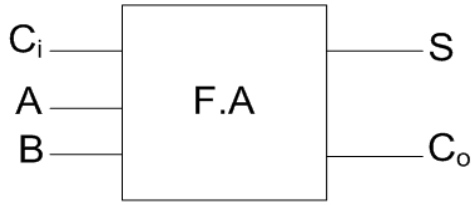


Fig. 4.2. Full Adder (FA) symbol

Where:

C_i: carry- in from the previous addition.
C_o: carry- out to the next addition.

The truth table for a full-adder (FA) is determined by the 8 possible combinations of the inputs A, B and C_i. The corresponding values of S and C_o is given in table (4.2) from which we may write

Table 4.2: Truth Table of Full Adder (FA)

Input			Output	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the truth table,

$$S = \overline{A} \cdot \overline{B} \cdot C_i + \overline{A} \cdot B \cdot \overline{C_i} + A \cdot \overline{B} \cdot \overline{C_i} + A \cdot B \cdot C_i \quad \ldots\ldots (4.4.a)$$

$$= \left(\overline{A} \cdot \overline{B} + A \cdot B\right) \cdot C_i + (\bar{A} \cdot B + A \cdot \bar{B}) \cdot \overline{C_i} = A \oplus B \oplus C \quad \ldots\ldots (4.4.b)$$

$$C_o = \overline{A} \cdot B \cdot C_i + A \cdot \bar{B} \cdot C_i + A \cdot B \cdot \overline{C_i} + A \cdot B \cdot C_i \quad \ldots\ldots (4.5.a)$$

$$= A \cdot B + C_i(A \oplus B) \quad \ldots\ldots (4.5.b)$$

Procedure:

1- Implement Half Adder (HA) using logic.ly then verify the truth table.

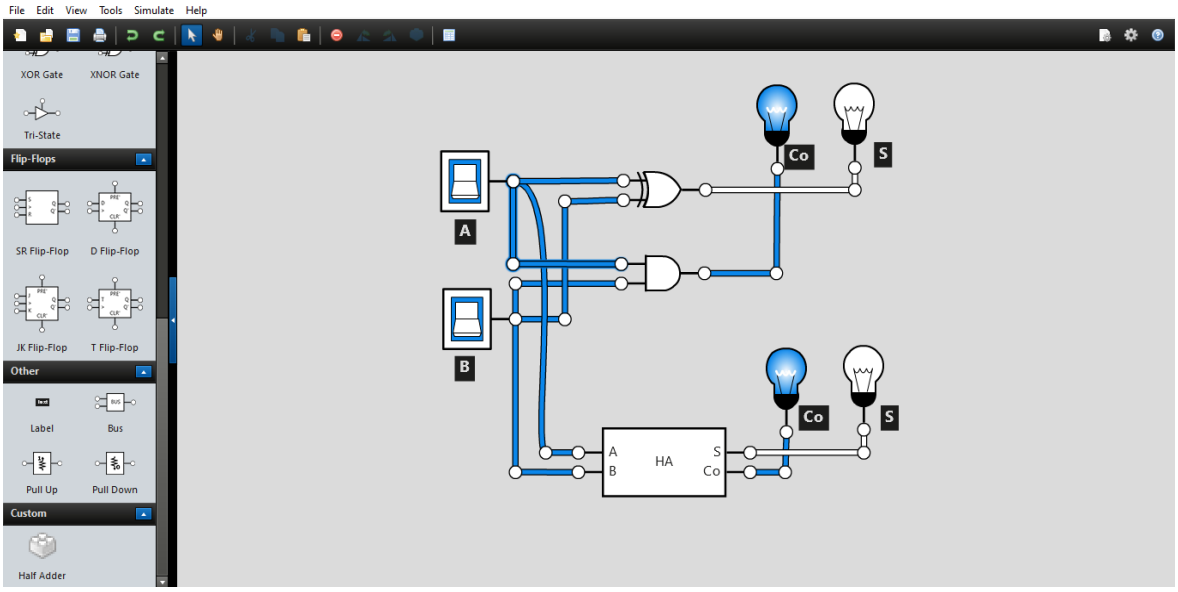


Fig. 4.3. Implementation of HA using Logic.ly

2- Implement Full Adder (FA) using logic.ly then verify the truth table.

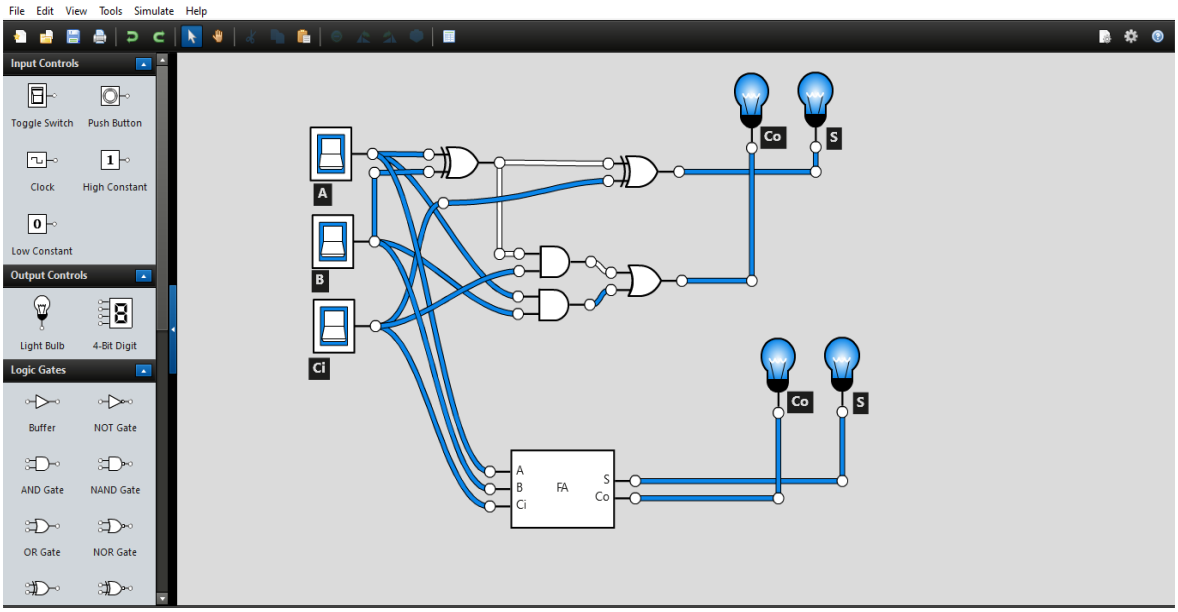


Fig. 4.4. Implementation of FA using Logic.ly

3- Implement a binary parallel adder circuit of 2-bit using Full Adder (FA) blocks only then verify the truth table. (***This circuit represents 7482 IC***).

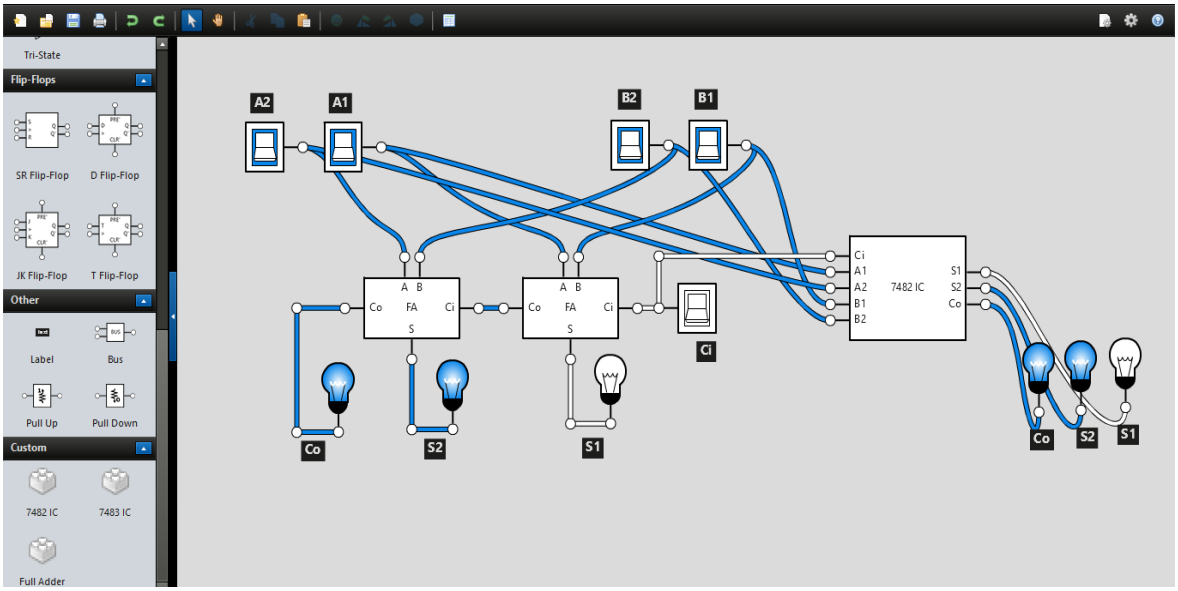


Fig. 4.5. Binary parallel adder of 2-bit using Logic.ly

4- Implement a binary parallel adder circuit of 4-bit using Full Adder (FA) blocks only then verify the truth table. (***This circuit represents 7483 IC***).

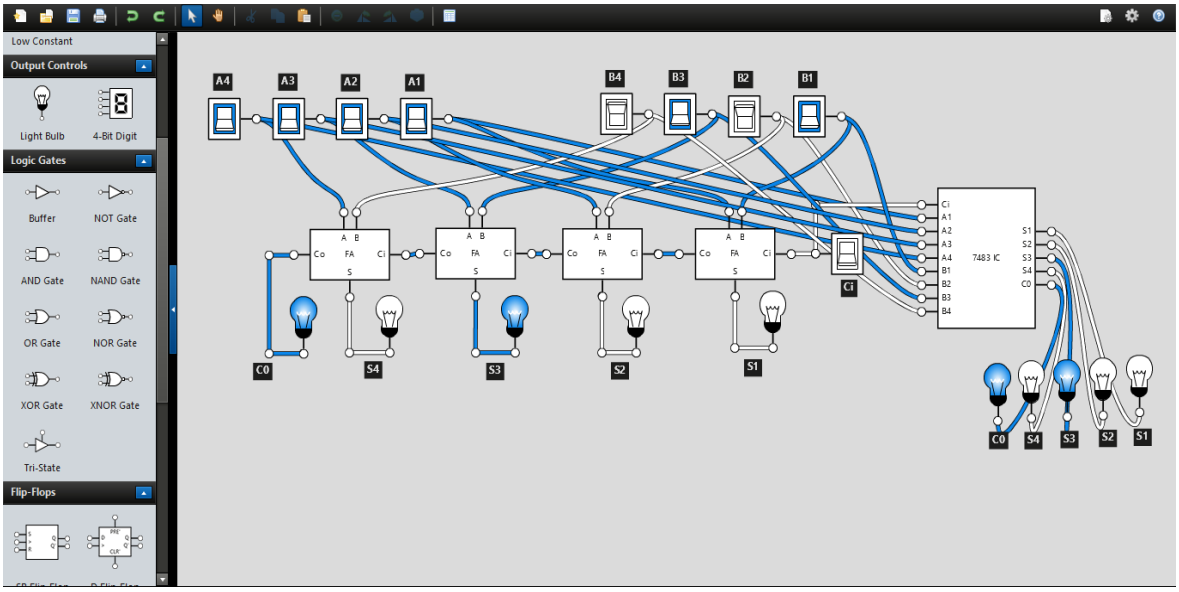


Fig. 4.6. Binary parallel adder of 4-bit using Logic.ly

Discussion:

1. Design FA by means of HA blocks and one OR gate only.
2. Design FA using two 2-input EX-OR and three 2-input NAND gates only.
3. Add a two binary numbers 110 & 111 using FA blocks only.
4. Add a two binary numbers 10110 & 10111 using 7482 and 7483 ICs only.
5. Add a two binary numbers 110010 & 100101 using 7483 ICs only.
6. What is the operation of the following logic circuit.