First Exam, M.P.A. Date: 24/3/2019 Class: Year2 /Evening study

Q1/ Select the correct answers ***for 5*** from the following:

1. **What is the** function of the chip select line (CS') in a memory chip?
   a. Power supply is applied to the chip when CS' is activated.
   b. The data bus will not be activated when CS' is deactivated.
   c. It prevents two or more subsystems from using the memory simultaneously.
   d. None of the above.

2. **Assume that** a 1G x 1 DRAM memory cell array is organized as **1M** rows and **1K** columns. The number of address bits required to select **a row** and **a column** will be:
   a. 20 and 10
   b. 30 and 1
   c. 220 and 210
   d. None of the above

3. **CSIC, RSIC, ASIC are types of:**
   a. Combination circuits that used to make CPU.
   b. Microprocessor types.
   c. Multiplexers which are important in microprocessor design.
   d. None of the above

4. **To build a 1G x 16 memory** system, the number of 256M x 8 module require are -------, with -----chips inside each module.
   a. 16 with 2.
   b. 23 with 1.
   c. 8 with 2.
   d. None of the above .

5. **Memory could** be expands
   a. Horizontal expansion only that mean which mean increase number of data
   b. Vertical expansion by increase no. of address line
   c. both of above
   d. None of the above

6- **Which of the following** statements are true?
   a. The main objective for using cache memory is to increase the effective speed of the memory system.
   b. Main memory is faster as compared to cache memory.
   c. The size of main memory is larger as compared to cache memory.

Q/2 Answer the following

1- How many address lines and input-output data lines are needed in each of the following memory units : (a) 4G X 64 ; (b) 64K x 8.

Correct answer are: (a) 32 address lines, 64 data lines (b) 16 address lines, 8 data lines

2-How many 128 **B**x 8 memory chips are needed to provide a memory capacity of 4096 **B** x 16 ? (Hint : $4096=2^{12}=4K$)

No. of chips needed= $(2^{12}x2^4)/2^7x2^3)=2^6=64$ chips

3- An array of two integers (an integer is 64 bits wide) is placed in memory starting with address 100 (the memory is byte addressable). Full in the blank with correct expression to load second element of the array to R_3 Register .

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MVI R1, 100        (starting address in R1 base)
LOAD R2, 0(R1)     (load the first element of array)
LOAD R3, ____      (load the second element of array)
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Correct answer is $7(R_1)$

Q3- Select ***one only***:

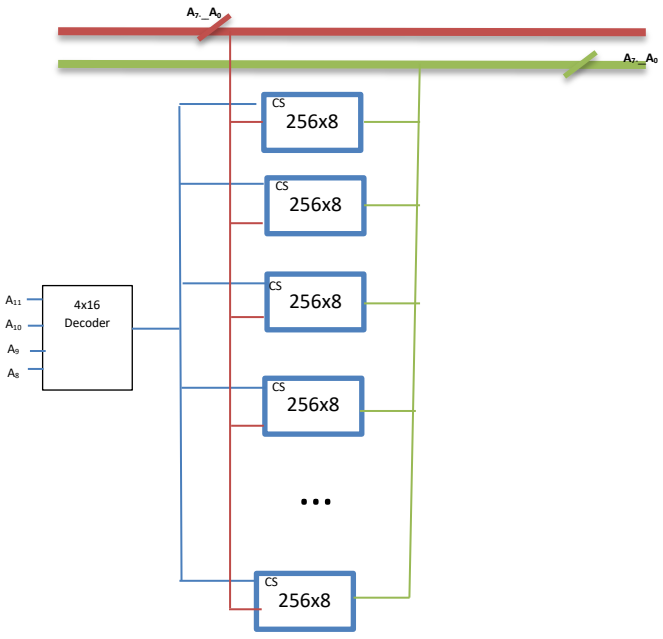
A/ Implement a memory with 4KB using 256BX 8 RAM chips. Draw the memory and determine effective addresses to be used?

No. of chips needed=$(2^{12}x2^3)/2^8x2^3)=16$ chips needed

No. of address lines for (4K)memory =12 bits , No. of address lines for (265)chip=8 bits ➔ 12-8=4 bits needed to address each chip.

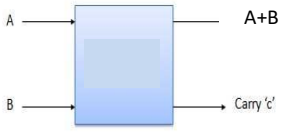
Effective address for 1st chip (000-0FF) Effective address for 2nd chip (100-1FF), ..etc (write all the EA)

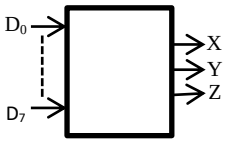
Drawing:

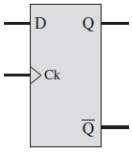


B/ For each of the following circuits, identify

a. Circuit Name and its role in computer architecture (where it use)
b. Give a truth table or property table for it (if found).







Half Adder (ALU) 8x3 Decoder (CPU) D Flip-Flop (Memory)

Inputs		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Refer to page 11 & 15 from Lecture 1