COMPUTERS ARCHITECTURE

Lecture 2

Multiplexers

Basic Concepts

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MULTIPLEXERS

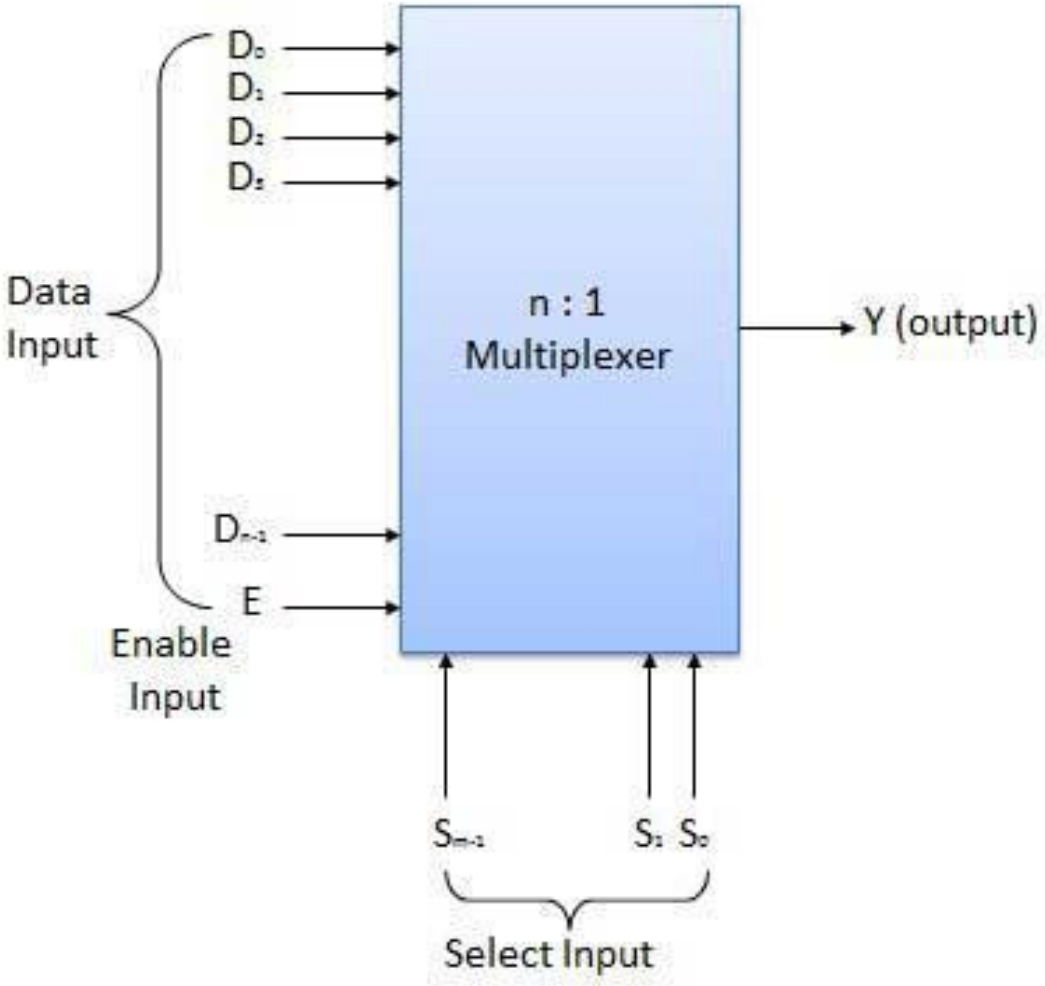
- Multiplexer is a ***special type of combinational circuit***. There are ***n-data*** inputs, ***one output*** and ***m*** select inputs with $2^m = n$

  It is a digital circuit which selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the selected inputs.

  Depending on the digital code applied at the selected inputs, one out of n data sources is selected and transmitted to the single output Y.

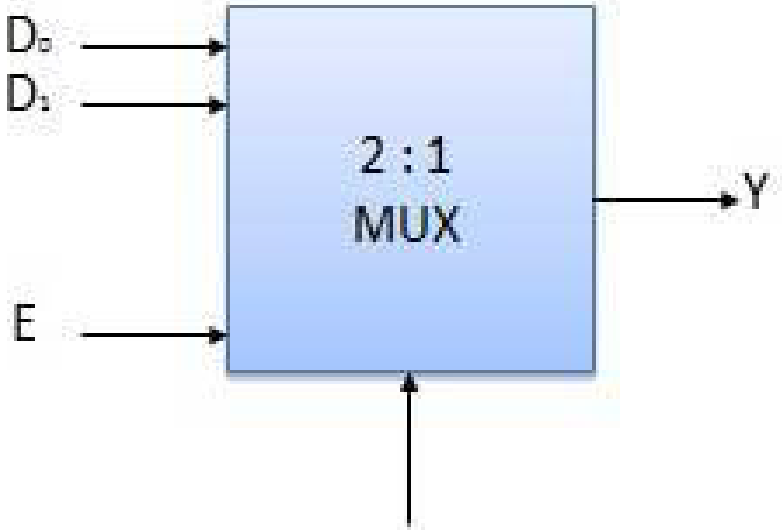
  E is called the enable input which is useful for the cascading. It is generally an active low terminal that means it will perform the required operation when it is low. Multiplexers come in multiple variations:

  2: 1 multiplexer; 4: 1 multiplexer; 16: 1 multiplexer; or 32 : 1 multiplexer


D0
D1
D2
D3
Data Input
n : 1 Multiplexer
Y (output)
Dn-1
E
Enable Input
Sm-1
S1
S0
Select Input

Enable	Select	Output
E	S	Y
0	x	0
1	0	D_0
1	1	D_1

x = Don't care



APPLICATIONS OF MULTIPLEXER:

- **Communication system** – Communication system is a set of system that enable communication like transmission system, relay and tributary station, and communication network.
- **Telephone network –** In telephone network, multiple audio signals are integrated on a single line for transmission with the help of multiplexers.
- **Computer memory** – Multiplexers are used to implement huge amount of memory into the computer, at the same time reduces the number of copper lines required to connect the memory to other parts of the computer circuit.
- **Transmission from the computer system of a satellite** – Multiplexer can be used for the transmission of data signals from the computer system of a satellite or spacecraft to the ground system using the GPS

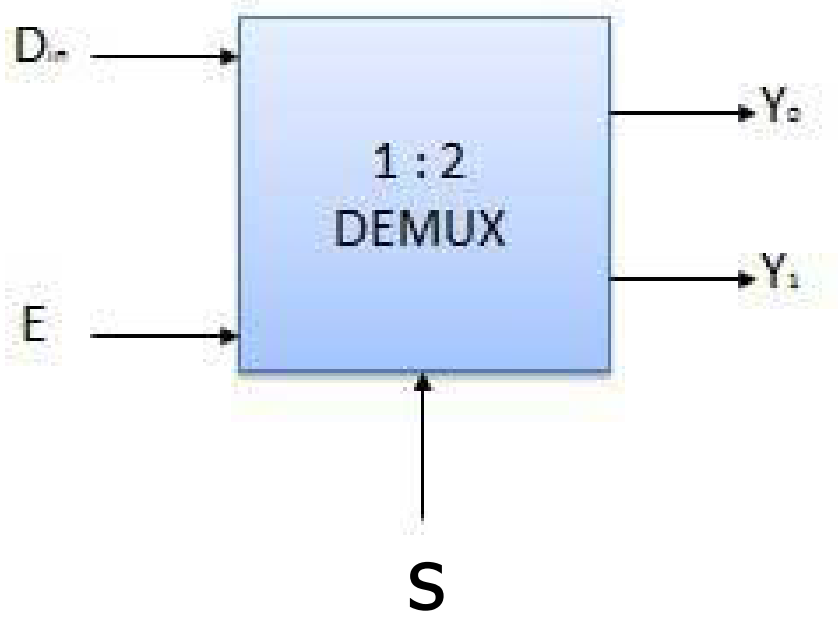
6.DE-MULTIPLEXERS

A de-multiplexer performs the reverse operation of a multiplexer i.e. it receives one input and distributes it over several outputs. It has only one input, n outputs, m select input. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line. A de-multiplexer is equivalent to a single pole multiple way switch as shown in fig.

De-multiplexers come in multiple variations. 1 : 2 demultiplexer.; 1 : 4 demultiplexer. ; 1 : 16 demultiplexer; 1 : 32 demultiplexer

Enable	Select	Output	
E	S	Y0	Y1
0	x	0	0
1	0	0	D_{in}
1	1	D_{in}	0

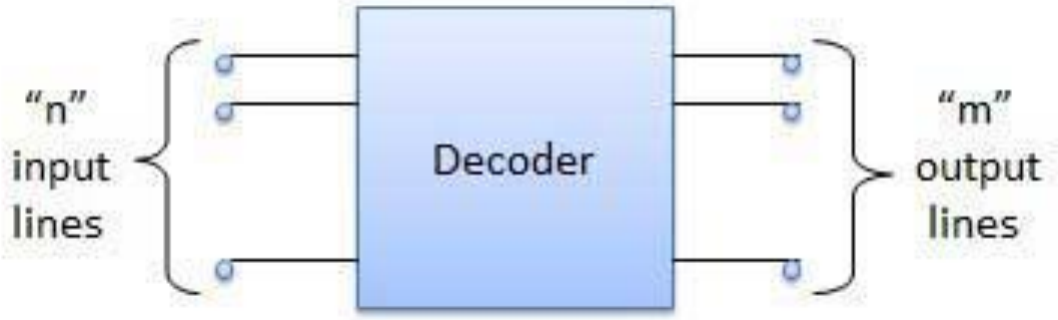
x = Don't care



DECODER

- A decoder is a combinational circuit. It has **n** input and to a maximum m= 2^n outputs. Decoder is identical to a de-multiplexer without any data input.

  It performs operations which are exactly opposite to those of an encoder.



Examples of Decoders are: Code converters and BCD to seven segment decoders.

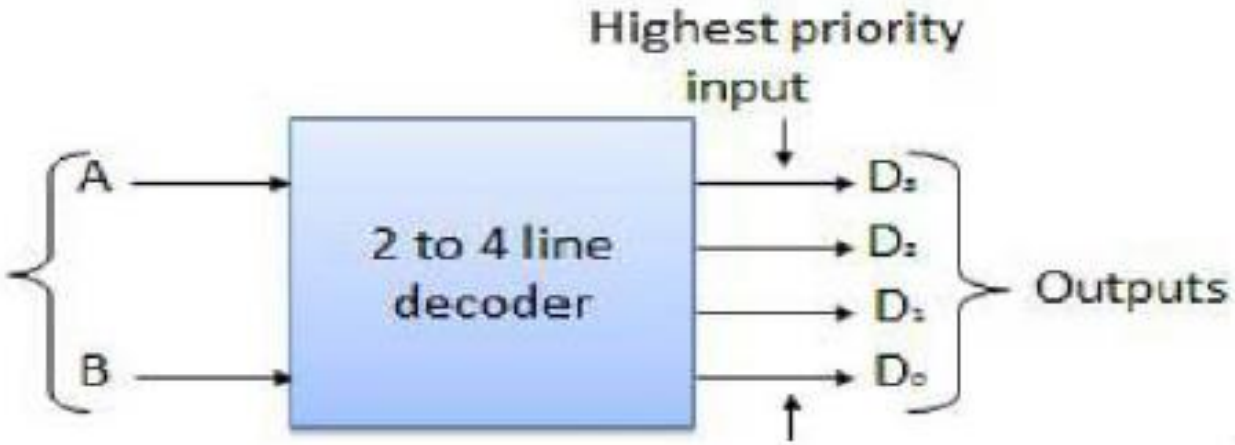
2 to 4 Line Decoder

The block diagram of 2 to 4 line decoder is shown in the fig.

A and B are the two inputs where D0 through D3 are the four outputs.

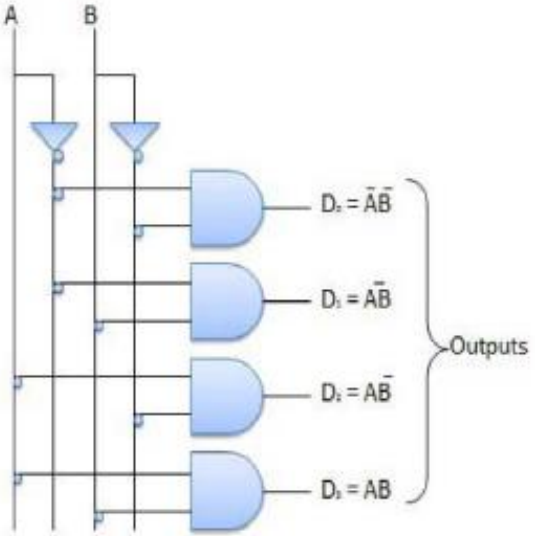
Truth table explains the operations of a decoder.

It shows that each output is 1 for only a specific combination of inputs.



Inputs		Output			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Truth Table

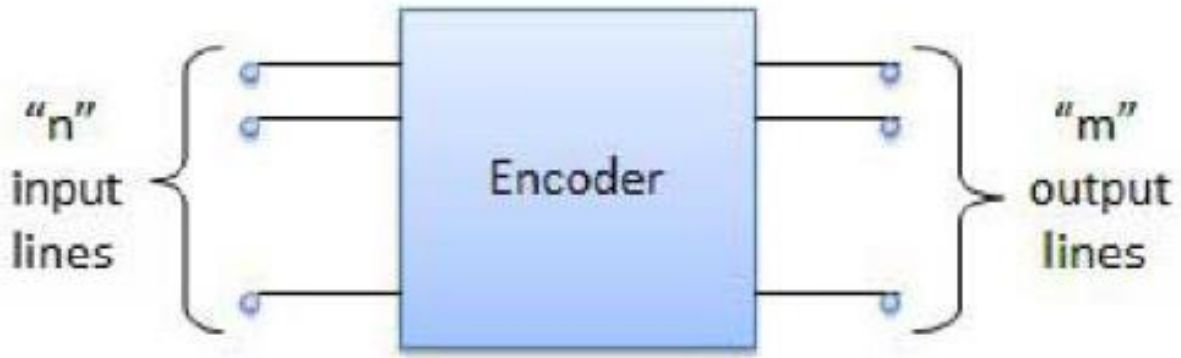


Logic Circuit

ENCODER

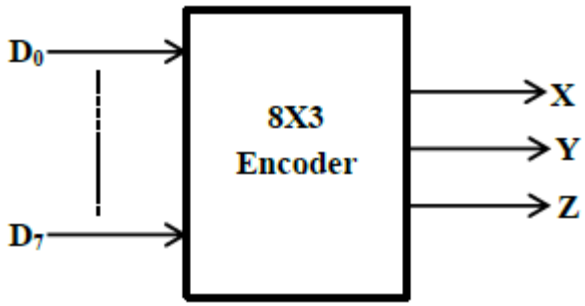
Encoder is a combinational circuit which is designed to perform the inverse operation of the decoder. An encoder has **n** number of input lines and **m** number of output lines. An encoder produces an **m** bit binary code corresponding to the digital input number. The encoder accepts an **n** input digital word and converts it into an **m** bit another digital word.

Examples of Encoders are: Decimal to BCD encoder; Octal to binary encoder; Hexadecimal to binary encoder; etc.



As an example:
let's consider octal to binary encoder. As shown in the following figure, an octal-to-binary encoder takes 8 input lines and generates 3 output lines

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1



As seen from the truth table, the output is 000 when D0 is active; 001 when D1 is active; 010 when D2 is active and so on.

H.W/

1. Give the internal logic gate for the 1:4 DeMax?

2. Design a 8:3 Encoder with enable line?

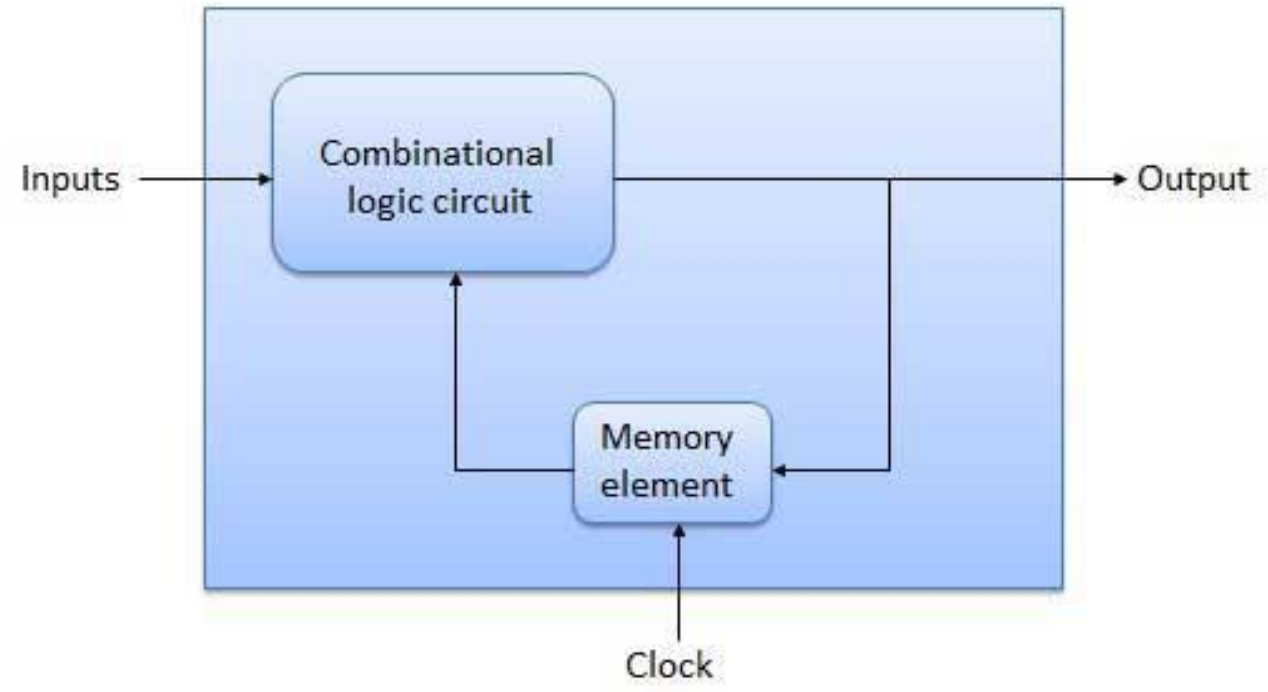
3. Design a full adder using

1) Half Adder circuit
2) 3:8 decoder and 2 OR gate
3) 8:1 Max's

SEQUENTIAL CIRCUITS

The ***combinational*** circuit does not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit.

But ***sequential*** circuit has memory so output can vary based on input. This type of circuits uses ***previous input, output, clock and a memory element.***



Combinational circuits implement the essential functions of a digital computer.

1. The current output of a sequential circuit depends not only on the current input, but also on the past history of inputs.
2. the current output of a sequential circuit depends on the current input and the current state of that circuit.
3. the sequential circuit makes use of combinational circuits.

FLIP FLOP

A flip flop is an electronic circuit with ***two stable states*** that can be used to ***store binary data***. The stored data can be changed by applying varying inputs.

The simplest form of sequential circuit is the flip-flop. There are a variety of flip-flops, all of which share two properties:

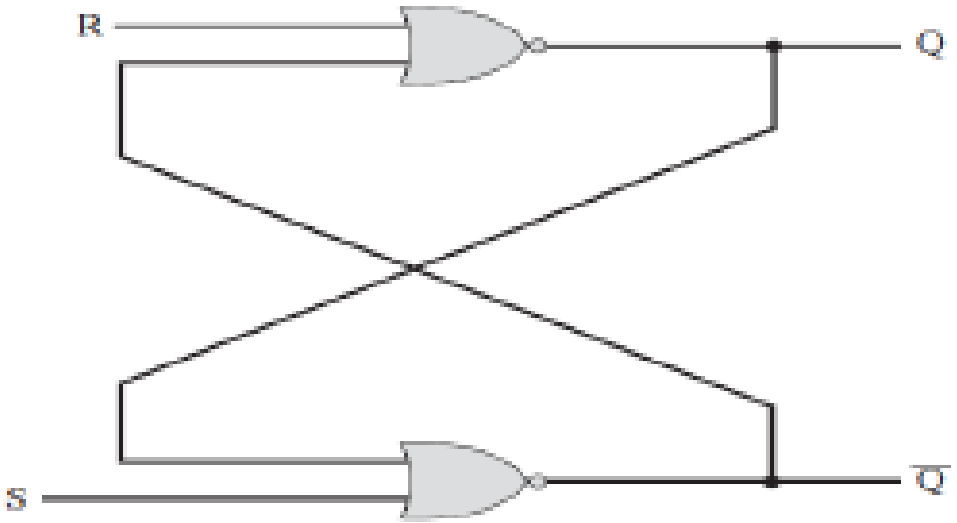
1. The flip-flop is a bistable device. It exists in one of two states, in the absence of input, remains in that state. Thus, the flip-flop can function as a 1-bit memory.
2. The flip-flop has two outputs, which are always the complements of each other.

These are generally labeled Q and Q

Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

THE S–R LATCH

Figure, shows a common configuration known as the S–R flip-flop or S–R latch. The circuit has two inputs, S (Set) and R (Reset), and two outputs, Q and consists of two NOR gates connected in a feedback arrangement.



The S–R latch can be defined with a table similar to a truth table, called a ***characteristic table***, which shows the next state (Q_n+1) or states of a sequential circuit as a function of current states (Q_n) and inputs.

S-R Truth Table

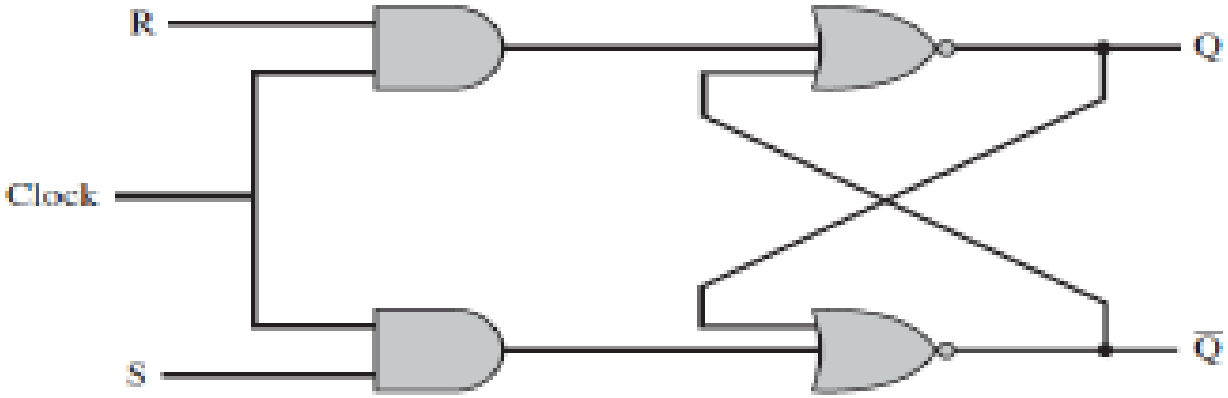
S	R	Q_{n+1}
0	0	No Change (Q_n)
0	1	0
1	0	1
1	1	Not allowed

characteristic table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	-
0	0	1	1
0	1	1	0
1	0	1	1
1	1	1	-

CLOCKED S–R FLIP-FLOP

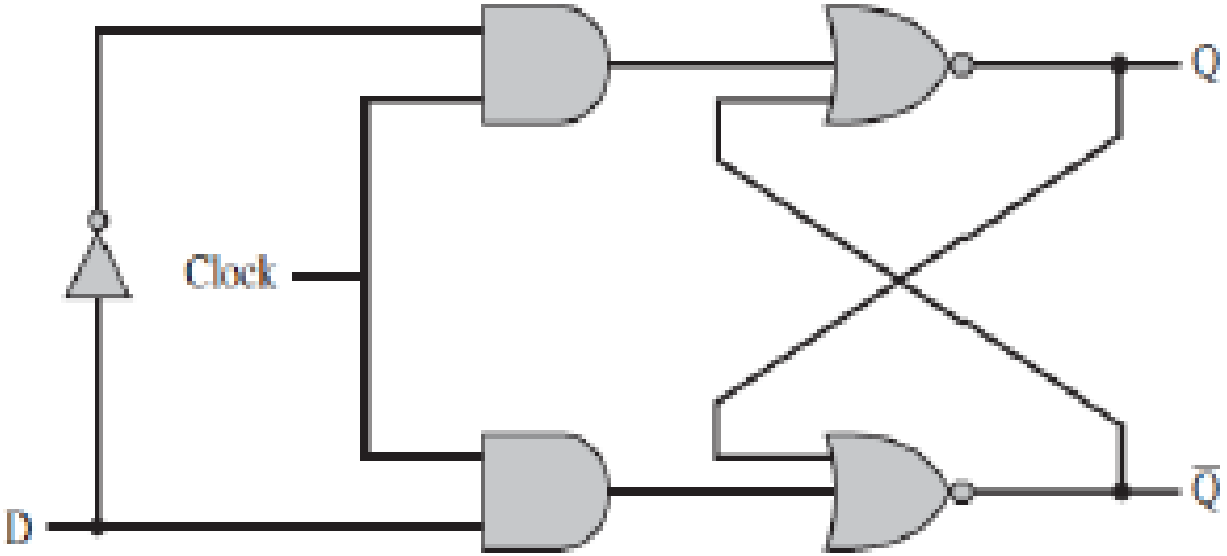
The output of the S–R latch changes, after a brief time delay, in response to a change in the input. This is referred to as asynchronous operation. More typically, events in the digital computer are synchronized to a clock pulse, so that changes occur only when a clock pulse occurs. Figure , shows this arrangement. This device is referred to as a *clocked S–R flip-flop*.



D FLIP-FLOP

One problem with S–R flip-flop is that the condition (R = 1, S = 1) must be avoided. One way to do this is to allow just a single input. The D flip-flop accomplishes this. By using an inverter, the non-clock inputs to the two AND gates are guaranteed to be the opposite of each other.

The D flip-flop is sometimes referred to as the data flip-flop because it is, in effect, storage for one bit of data. The output of the D flip-flop is always equal to the most recent value applied to the input.

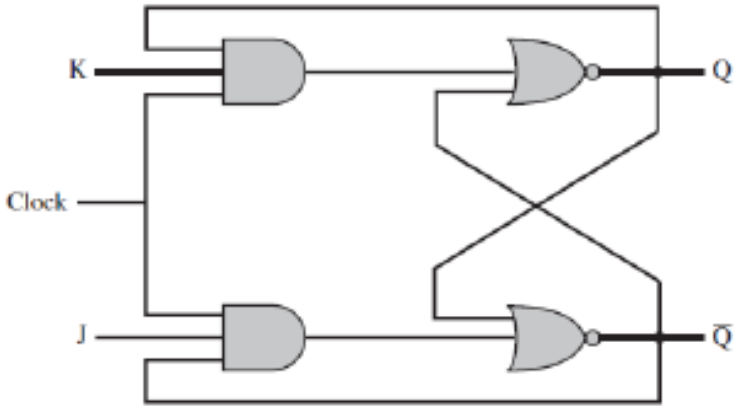


D	Q_{n+1}
0	0
1	1

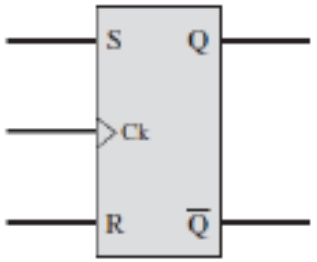
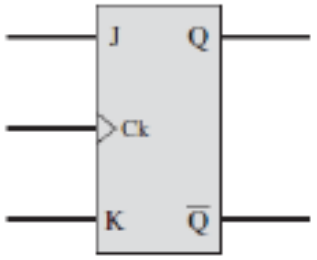
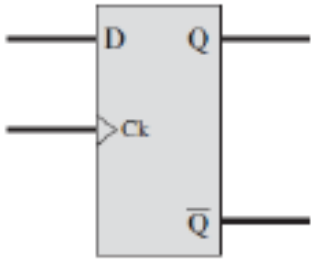
J–K FLIP-FLOP

- Another useful flip-flop is the J–K flip-flop. Like the S–R flip-flop, it has two inputs. However, in this case all possible combinations of input

J	K	Q_{n+1}
0	0	No Change (Q_n)
0	1	0
1	0	1
1	1	Toggle ($\overline{Q_n}$)



The following table shows the basic block diagram of S-R, J-K, and D Flip Flops with corresponding their truth table.

Name	Graphical Symbol	Truth Table
S–R		S R Q_{n+1} 0 0 Q_n 0 1 0 1 0 1 1 1 –
J–K		J K Q_{n+1} 0 0 Q_n 0 1 0 1 0 1 1 1 $\overline{Q_n}$
D		D Q_{n+1} 0 0 1 1