Chapter (2)

Field-Effect Transistor (FET)

Figures (2-4) and (2-8) represent transconductance curve of an n-channel JFET and EMOSFET transistors, respectively. There are multiple regions in the transconductance curve (between drain current (I_D) and gate-source voltage V_{GS}) as follows:

1) **Ohmic Region:**

   The only region in which transconductance curve shows linear response and drain current is opposed by the (JFET or EMOSFET) transistor resistance is termed as Ohmic region.

2) **Saturation Region**:

   In the saturation region, the n-channel (JFET or MOSFET) transistors are in ON condition and active, as maximum current flows because of the gate-source voltage applied.

3) **Cutoff Region**:

   In this cutoff region, there will be no drain current (I_D) flowing and thus, the transistors are in OFF condition.

4) **Breakdown Region:**

   If the VDS voltage applied to the drain terminal exceeds the maximum necessary voltage, then the transistor fails to resist the current, and thus, the current flows from the drain terminal to the source terminal. Hence, the transistor enters in the breakdown region.

2.6 Transconductance Curve of n-channel (JFET and EMOSFET)

2.6.1 n-channel JFET

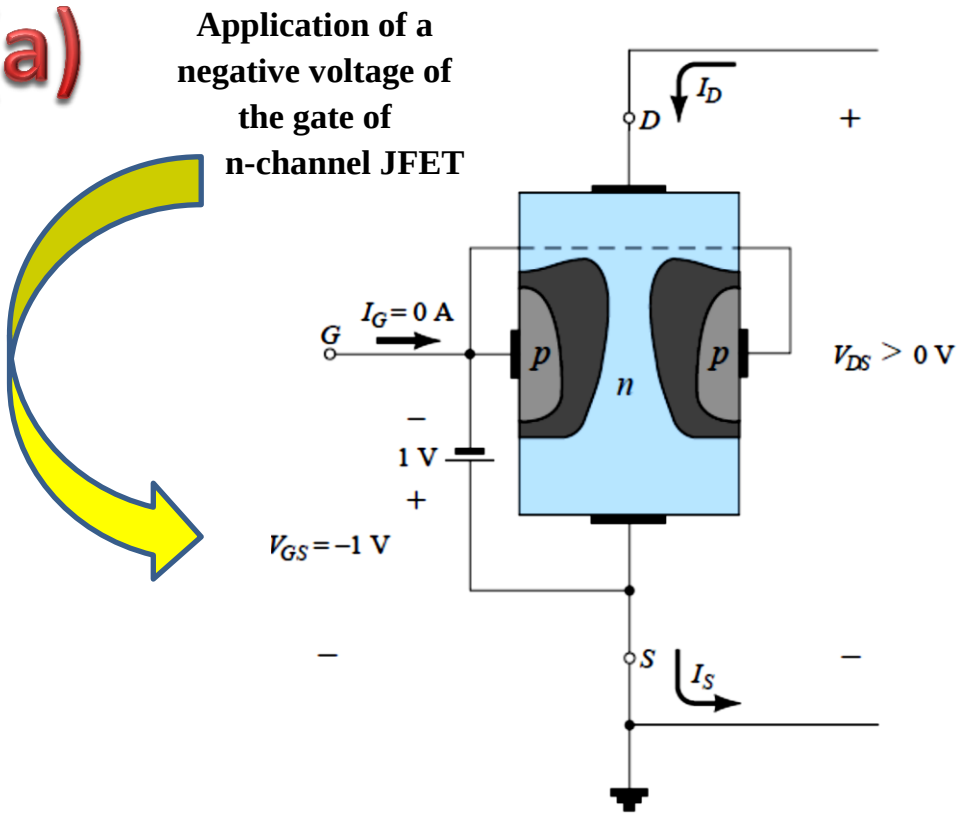
As the voltage V_{DS} is increased from (0 to a few volts), the drain current (I_D) will increase as determined by **Ohm's law** and the plot of (I_D) versus (V_{DS}) will appear as shown in Fig. 2-4. From the transconductance curve of n-channel JFET is showed in the Figs. (2-4 and 2-9), I_{DSS} is the maximum drain current for an n-channel JFET and is defined by the conditions V_{GS} = 0 V and $V_{DS} > V_P$ (where V_P is pinch-off voltage). As well as, I_D = 0 mA is defined by the conditions $V_{GS} = V_P$.

For example, in an n-channel JFET device the controlling voltage V_{GS} is made more and more negative from its V_{GS} = 0 V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source. Fig.2-9a-b shows that a negative voltage of (-1 V) has been applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with V_{GS} = 0 V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} as shown in Fig. 2-9b for V_{GS}= -1 V. The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative.

Note also on (Fig. 2-9) how the pinch-off voltage (V_P) continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Finally, V_{GS} when $V_{GS}=V_P$ will be sufficiently negative to establish a saturation level that is essentially (I_D = 0 mA), and for all practical purposes the device has been "turned off".

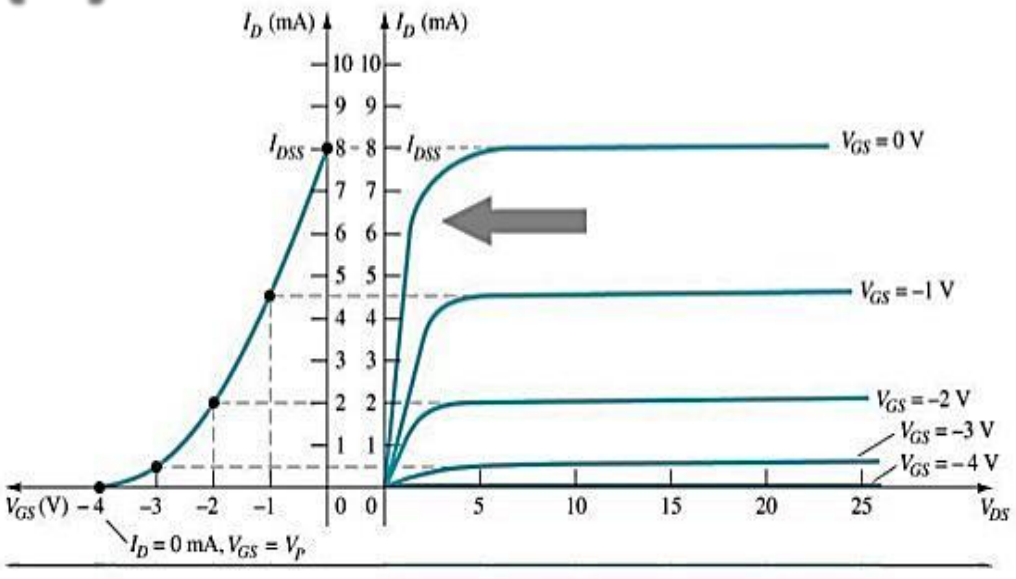
(a)

Application of a negative voltage of the gate of n-channel JFET



(b)

Transfer (Transconductance) Curve



(Figs. 2-9a-b): Diagram of n-channel JFET and their (I-V) characteristics.

2.6-2 n-channel EMOSFET

In n-channel enhancement-mode MOSFET (EMOSFET), when the gate bias voltage, V_{GS} is equal to zero (V_{GS} = 0) that results in the device being normally "OFF" (non-conducting). If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 2-10, the absence of an n-channel will result in a current of effectively zero amperes (I_D= 0 A). It is quite different from the n-channel depletion-mode MOSFET (DMOSFTE) and n-channel JFET where $I_D = I_{DSS}$ when (V_{GS} = 0).

That means, in an n-channel EMOSFET transistor a drain current will only flow when a gate voltage (V_{GS}) is applied to the gate terminal greater than the threshold voltage (V_T) level in which conductance takes place making it a transconductance device Fig. (2-7 and 2-10). The application of a positive (+ve) gate voltage to an n-type EMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel. Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, I_D through the channel. In other words, for an n-channel EMOSFET: $+V_{GS}$ turns the transistor "ON", while a zero or negative ($-V_{GS}$) turns the transistor "OFF".

The reverse is true for the p-channel enhancement MOSFET. When (V_{GS} = 0 V) the device is "OFF" and the channel is open. The application of a negative ($-V_{GS}$) gate voltage to the p-type EMOSFET enhances the channels

conductivity turning it "ON". Then for a p-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor "OFF", while $-V_{GS}$ turns the transistor "ON".

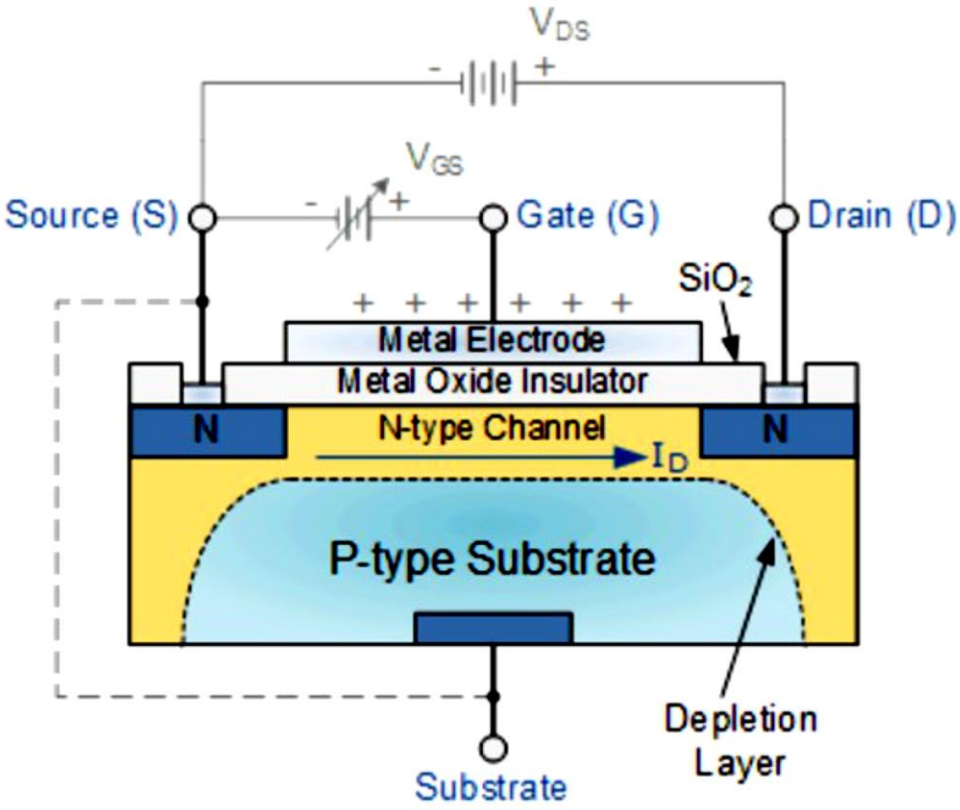


Fig. 2-10: n-channel enhancement-mode (EMOSFET)

As aforementioned, for values of V_{GS} less than or equal to the threshold level (V_T), the drain current (I_D) of an n-channel EMOSFET is (0 mA). Figure 2-4 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA.

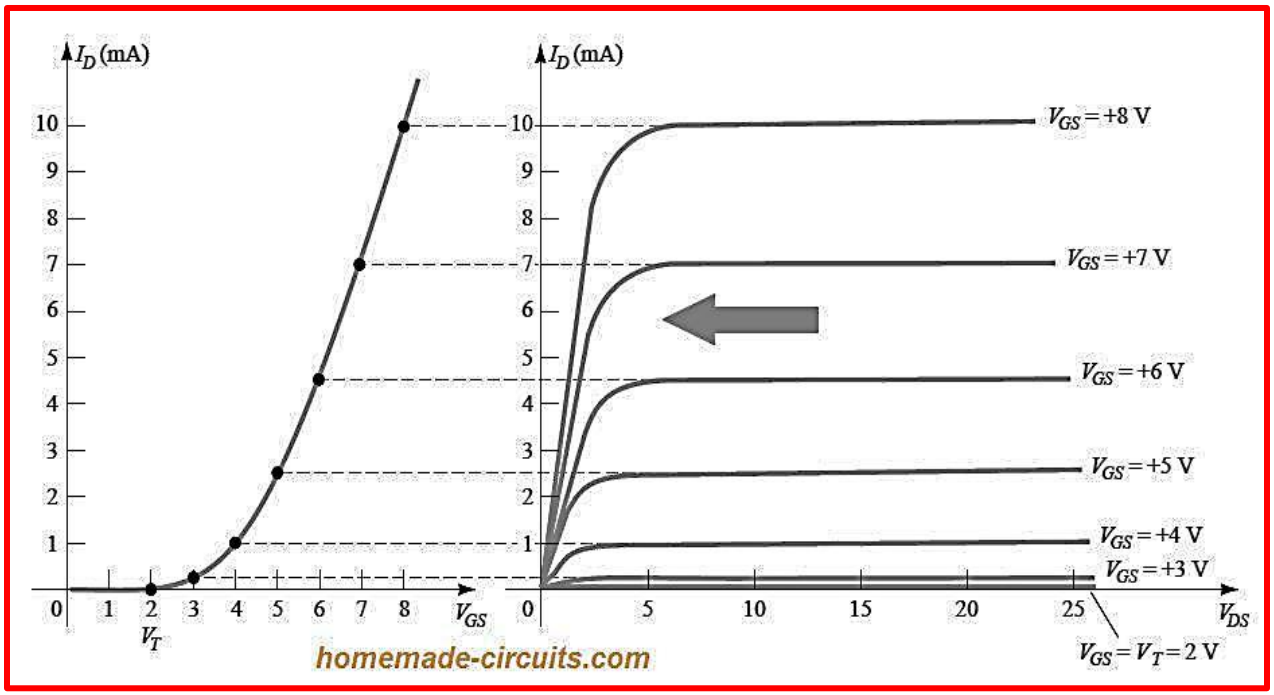


Fig 2-11: (I-V) characteristics for n-channel EMOSFET.