Lecture 4
Computer Technology

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Lecture 4
Microcomputer Architecture

A computer system has three main components:
1. Central Processing Unit (CPU) or processor,
2. Memory Unit
3. Input/output Units (devices).

4.1 Personal Computer (PC) Components:-

The main component of the PC is ***System Board*** (or ***motherboard***). It contains the ***processor***, ***main memory***, ***connectors***, and ***expansion slots*** for ***optional cards***.

a) **The slots and connectors** provide access to such components as ROM, RAM, hard disk, CD-ROM drive, additional memory, video unit, keyboard, mouse, parallel and serial device, sound adapter and cache memory (the processor use high speed cache memory to decrease its need to access the slower main memory).

b) **A bus** with wires attached to the system board connects the components. It transfers data between the processor, memory and external devices.

4.1.1 The processor

The CPU or processor acts as the controller of all actions or services provided by the system. The operations of a CPU can be reduced to three basic steps: **fetch**, **decode**, and **execute**. Each step includes intermediate steps, some of which are:

1- Fetch the next instruction:
- Place it in a holding area called a queue.
- Decode the instruction.

2- Decode the instruction
- Perform address translation.
- Fetch operand from memory.

3- Execute the instruction.
- Perform the required calculation.
- Store results in memory or register.
- Set status flag attached to the CPU.

4.1.2 System Bus

The components of the computer system must communicate with each other and with the outside world. Although it may be possible to connect each component to the CPU separately as a practical matter this would require too many physical connects. To keep the number of connections manageable, the processor is connected to memory and all peripherals using a bus.

A Bus is a bunch of wires, and electrical path on the printed IC to which everything in the system is connected. There are three types of Bus:

1. **Address Bus (AB):** the width of AB determines the amount of physical memory addressable by the processor.

2. **Data Bus (DB):** the width of DB indicates the size of the data transferred between the processor and memory or I/O device.

3. **Control Bus (CB):** consists of a set of control signals, typical control signals includes memory read, memory write, I/O read, I/O write, interrupt acknowledge, bus request.

These control signals indicates the type of action taking place on the system us.

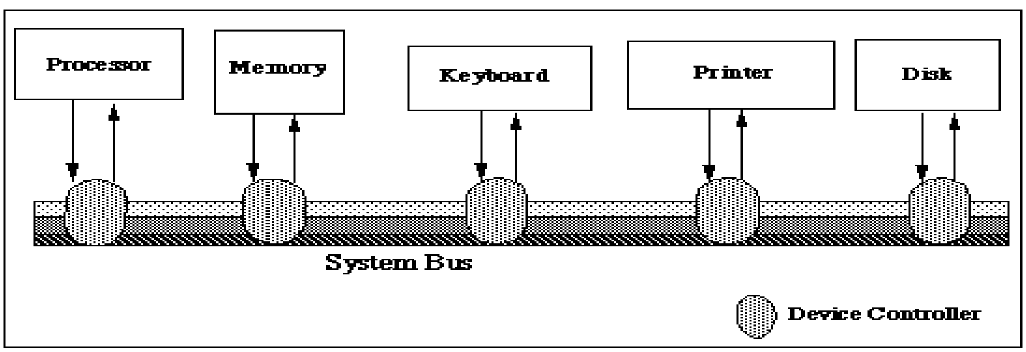

Figure (1) The system bus:

the processor communicates with all devices via the system bus

The CPU is divided into two general parts. **Arithmetic Logic Unit** (ALU) and **Control Unit** (CU).

- The **ALU** carry Arithmetic, logical, and shifting operations.
- The **CU** fetches data and instruction, and decodes addresses for the ALU.

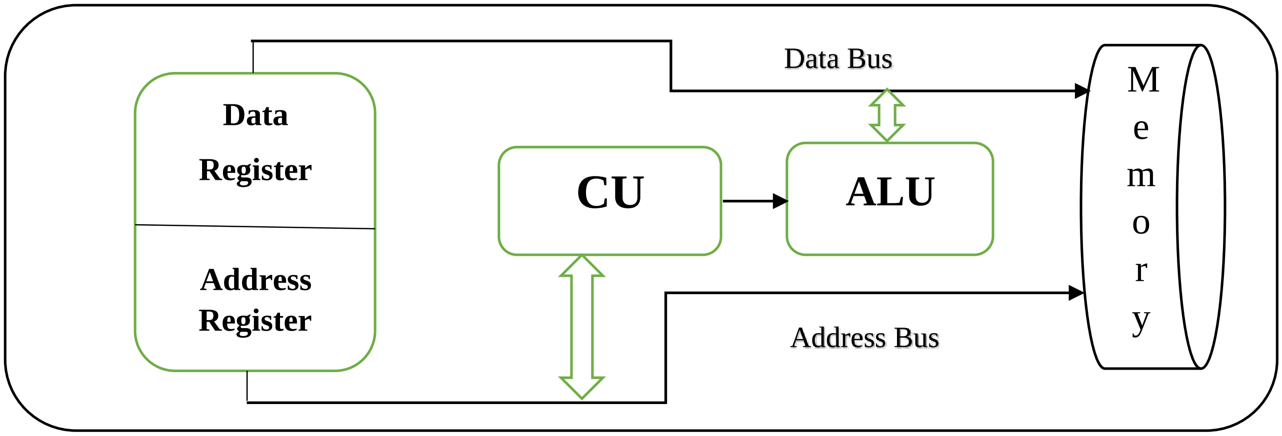

Figure **(2): A Block Diagram of the Simple CPU**

2.1.3 Register

Registers are devices capable of storing information, receiving data from other areas within the computer and transferring information as directed by the control unit, it is used for temporary storage of data or instruction and the most important register are:

1. **Program counter** (PC): hold address of the next instruction.
2. **Instruction register** (IR): Hold instruction while it is decoded and Executed
3. **Address register** (AR): holds the address of memory location.
4. **PSW** (Processor Status Word): collection of bits called Flags or Condition Codes. They typical used to indicate a Zero result, a Negative result, a Carry, an Overflow and so on.
5. **SP** (Stack Pointer): Stack may consist of a set of internal registers or a portion of main memory. It is used for temporarily storing important information while subroutines are being executed. The top of the stack is the last information put onto the stack.

The instruction is brought in from the memory and placed in the IR. The Control Unit then decodes the instruction direct its execution. At the same time the CU sets the PC/IP to the address of the next instruction.

4.1.2 Memory (Main Memory)

The memory of a computer system consist of tiny electronic switches, with each switch set in one of two states: open or close. It is however more convenient to think of these states **as 0 and 1**.Thus each switch can represent a binary digit or bit, as it is known, the memory unit consists of millions of such bits, bits are organized into groups of eight bits called **byte**. Memory can be viewed as consisting of an ordered sequence of bytes. Each byte in this memory can be identified by its sequence number starting with 0, as shown in Figure 3. This is referred to as memory address of the byte. Such memory is called **byte addressable memory.** The memory address space of a system is determined by the address bus width of the CPU used in the system.

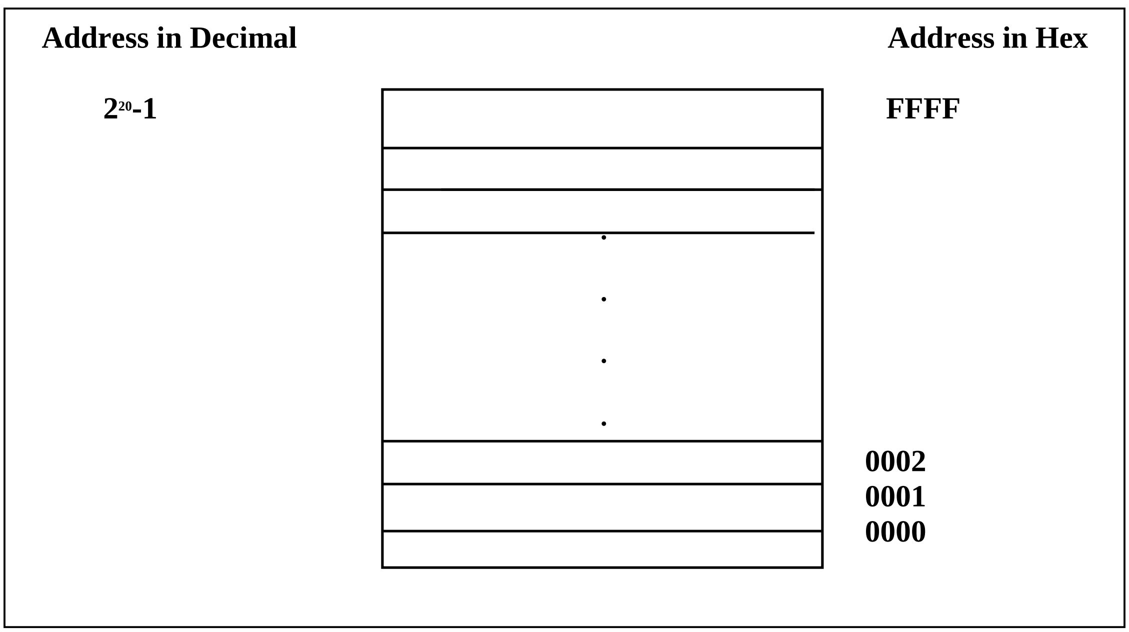

Figure 3: Logical view of the system memory

Two basic memory operations

The memory unit supports two fundamental operations: ***Read*** and ***Write***. The read operation read a previously stored data and the write operation stores a value in memory.

Steps in a typical ***read cycle***

1. Place the address of the location to be read on the address bus.
2. Activate the memory read control signal on the control bus.
3. Wait for the memory to retrieve the data from the address memory location.
4. Read the data from the data bus.
5. Drop the memory read control signal to terminate the read cycle.

Steps in a typical ***write cycle***

1. Place the address of the location to be written on the address bus.
2. Place the data to be written on the data bus.
3. Activate the memory write control signal on the control bus.
4. Wait for the memory to store the data at the address location.
5. Drop the memory write control signal to terminate the write cycle.

Addresses

Group of bits which are arranged sequentially in memory, to enable direct access, a number called address is associated with each group. Addresses start at 0 and increase for successive groups. The term location refers to a group of bits with a unique address. Table 1 represents Bit, Byte, and Larger units.

Table1: Bit, Byte, and Larger units.

Name	Number of Byte
Bit	0 or 1
Byte	is a group of bits used to represent a character, typically 8-bit.
Word	2-byte (16-bit)
Double Word	4-byte (32-bits)
Quadword	8-byte (64-byte)
Paragraph	16-byte (128-bit)
Kilo Byte (KB)	The number 2^{10}=1024=1 KB thus 640K=640*1024=655360 bytes)
Megabyte (MB)	(1024*1024) byte or 1,048,576 byte) approximately 1,000,000 bytes
Gigabyte (GB)	(1024*1024*10240byte) or (1,073,741,824 byte), approximately 1,000,000,000 bytes.
Terabyte (TB)	Approximately 1,000,000,000,000 bytes.

Memory chips

Memory chips have two main properties that determine their application, storage capacity or size and access time or speed. A memory chip contains a number of locations, each of which stores one or more bits of data known as its bit width. The storage capacity of a memory chip is the product of the number of locations and the bit width. For example, a chip with 512 locations and a 2-bit data width has a memory size of 512×2=1024 bits.

Since the standard unit of data is a byte (8 bits), the above storage capacity is normally given as 1024/8 =128 bytes. The number of locations may be obtained from the address width of the chip. For example, a chip with 10 address lines has 2^{10}= 1024 or 1 k locations. Given an 8-bit data width, a 10- bit address chip has a memory size of $2^{10} \times 8 = 1024 \times 8 = 1k \times 1$ byte = 1 KB.

The computer's word size can be expressed in bytes as well as in bits. For example, a word size of 8-bit is also a word size of one byte; a word size of 16- bit is a word size of two byte. Computers are often described in terms of their word size, such as an 8-bit computer, a 16-bit computer and so on.

For example, a 16-bit computer is one in which the instruction data are stored in memory as 16-bit units, and processed by the CPU in 16-bit units. The word size also indicates the size of the data. Bus which carries data between the CPU and memory and between the CPU and I/O devices. To access the memory, to store or retrieve a single word of information, it is necessary to have a unique address. The word address is the number that identifies the location of a word in a memory.

Each word stored in a memory device has a unique address. Addresses are always expressed as binary number, although hexadecimal and decimal numbers are often used for convenience. The second properties of memory chips is access time, access time is the speed with which a location within the memory chip may be made a variable to the data bus. It is defend as the time interval between the instant that an address is sent to the memory chip and the instant that the data stored in to the location appears on the data bus. Access time is given in nanosecond (ns) and varies from 25 ns to the relatively slow 200 ns.

NOTS:

- The large computer (mainframes) have word-sizes that are usually in the 32-to-64 –bits range.

- Mini computers have a word sizes from 8-to-32-bits range.

- Microcomputers have a word sizes from 4-to-32-bits range.

In general a computer with a larger word size can execute programs of instruction at a fast rate because more data and more instruction are stuffed into one word. The larger word sizes, however, mean more lines making up the data bus, and therefore more interconnections between the CPU and memory and I/O devices.

The word size is 4-bit therefore there are 4-data I/P lines and 4data O/P lines. This memory has 32 different words, and therefore has 32 different addresses (storage location) from (00000) to(11111). Thus, we need a 5 address I/P lines.

Memory capacity = number of memory storage
Location ×size of each word
= (number of word) × (number of bits per word)
= m (word)*n (bits)
= m*n bits

The capacity of memory depends on two parameters, the number of words (m) and the number of bits per word (n). Every bit added to the length of address will double the number of words in the memory. The increase in the number of bits per bits requires that an increase the length of data I/P and data O/P lines.