Lecture 9
Computer Technology

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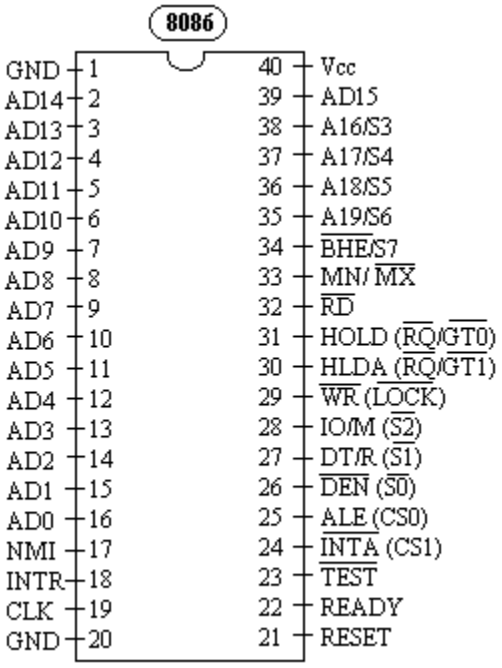
Lecture 9

An Introduction to 8086 Microprocessor Architecture

The 8086 is a 16-bit microprocessor chip designed by Intel in 1978, which gave rise to the x86 architecture. It has 20-bit address bus and 16-bit data bus.



9.1 Address / Data Bus

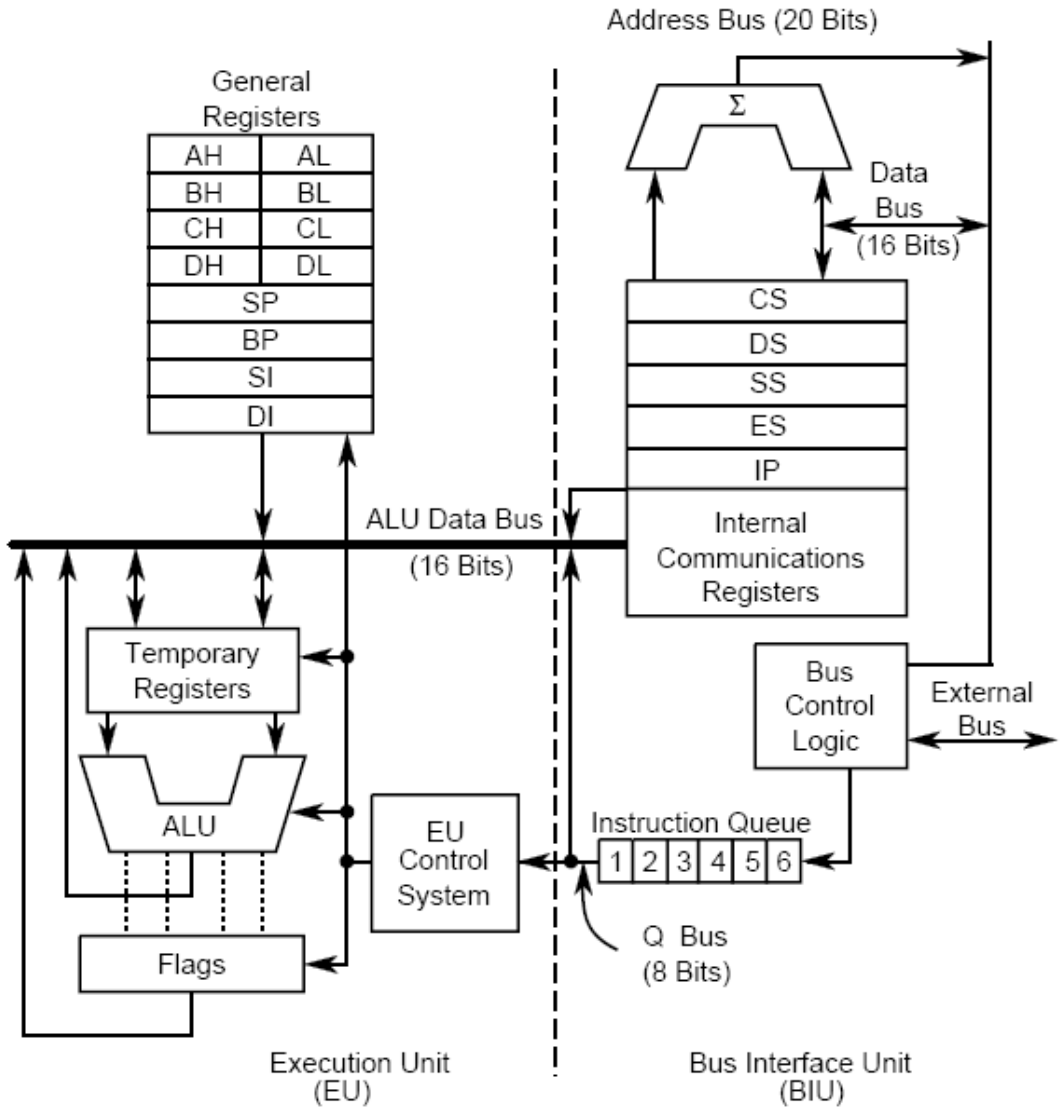
The address bus is 20-bit (A0-A19). A 20-bit address gives the 8086 a one Mega Byte memory address space. Moreover, it has an independent I/O address space, which is 64KB in length.

The 16-bit data bus lines D0-D15 are actually multiplexed with address lines A0-A15.

9.2 Internal Architecture of the 8086 MP

The 8086 Microprocessor Core incorporates two separate processing units: an **Execution Unit (EU)** and a **Bus Interface Unit (BIU)**. The Execution Unit is functionally identical among all family members.

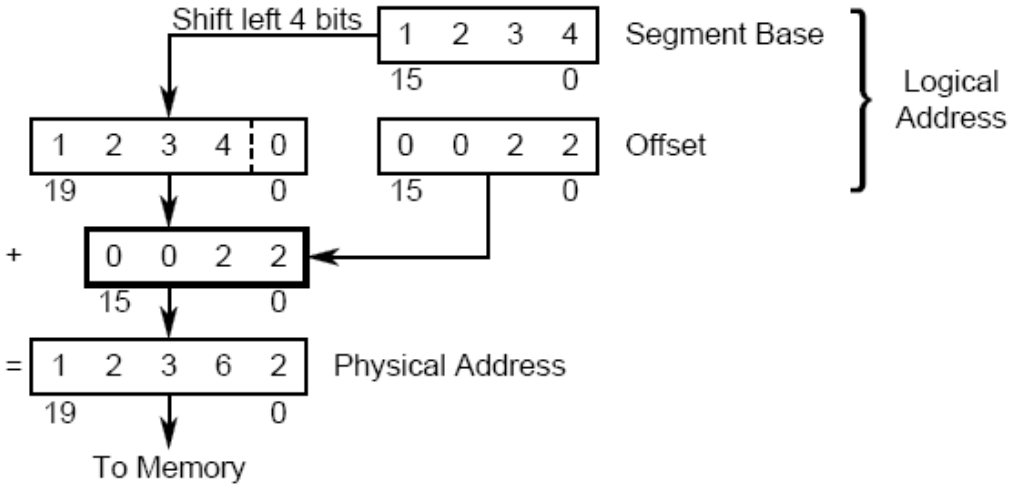
The Bus Interface Unit is configured for a 16-bit external data bus for the 8086 core. The two units interface via an instruction prefetch queue.



9.3 Bus Interface Unit

The Bus Interface Unit executes all external bus cycles. This unit consists of the segment registers (CS, DS, SS and ES) allow simple memory partitioning to aid modular programming, the Instruction Pointer (IP), the instruction code queue and several miscellaneous registers. The Bus Interface Unit transfers data to and from the Execution Unit on the ALU data bus.

The Bus Interface Unit generates a 20-bit physical address in a dedicated adder. The adder shifts a 16-bit segment value left 4 bits and then adds a 16-bit offset. This offset is derived from combinations of the pointer registers, the Instruction Pointer and immediate values. Any carry from this addition is ignored.



Physical Address Generation

During periods when the Execution Unit is busy executing instructions, the Bus Interface Unit sequentially prefetches instructions from memory. As long as the prefetch queue is partially full, the Execution Unit fetches instructions. BIU is also

responsible for generating bus control signal such as those for memory Read/Write and I/O Read/Write.

9.4 Execution Unit

The Execution Unit executes all instructions, provides data, addresses to the Bus Interface Unit, and manipulates the general registers and the Processor Status Word. The 16-bit ALU within the Execution Unit maintains the CPU status and control flags and manipulates the general registers and instruction operands. All registers and data paths in the Execution Unit are 16 bits wide for fast internal transfers. The Execution Unit does not connect directly to the system bus. It obtains instructions from a queue maintained by the Bus Interface Unit. When an instruction requires access to memory or a peripheral device, the Execution Unit requests the Bus Interface Unit to read and write data. Addresses manipulated by the Execution Unit are 16 bits wide. The Bus Interface Unit, however, performs an address calculation that allows the Execution Unit to access the full megabyte of memory space. To execute an instruction, the Execution Unit must first fetch the object code byte from the instruction queue and then execute the instruction. If the queue is empty when the Execution Unit is ready to fetch an instruction byte, the Execution Unit waits for the Bus Interface Unit to fetch the instruction byte.