

**Register transfer:**

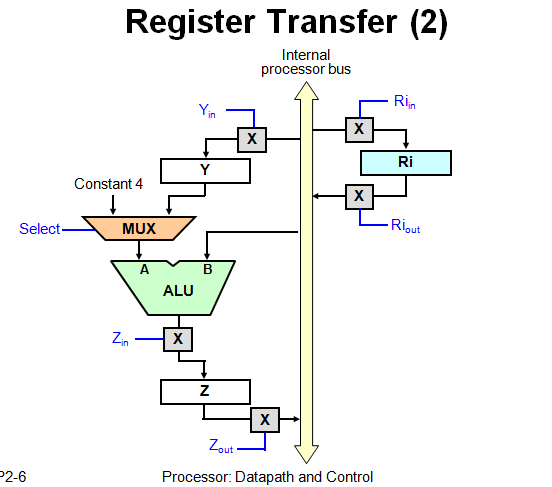
For each register Ri, there are two control signals:

Riin used to load the data on the bus into the register.

Riout used to place the register’s contents on the bus.

**EX**: R1 → R4 will be

R1out , R4in



**To perform arithmetic/logic operation:**

**.**The ALU is a combinational circuit that has no internal storage.

**.**ALU gets the two operands from MUX and bus. The result is temporarily stored in register Z.

**EX:** What is the sequence of operation to the following instruction:

ADD R1 , R2

**1.** R1out, Yin

**2.**R2out ,Select Y, Add, Zin

**3.**Zout ,R2in

**Fetching aword from memory:**

**EX:** MOVE (R1) ,R2

**1.** R1out ,MARin , Read

**2.** WMF( wait to memory function complete)

**3.** MDRout ,R2in

**Execution of a complete instruction:**

**EX:** Write the control steps to fetch and execute the following instruction:

ADD (R3), R1

Note: PCnew = PCold + constant 4

figure7

**Execution of Branch instructions:**

A branch instruction replaces the content of PC with the:

branch target address(PCnew)= offset **X** + PCold

offset **X** ( given in the branch instruction).

The required control steps to fetch and execute unconditional branch as follows:

1 PCout, MARin, Read, Select 4, Add, Zin

2 Zout, PCin, Yin, WMFC

3 MDRout, IRin

4 offset Xout,Select y, Add, Zin

5 Zout, PCin, End.

**EX:** The required control steps to fetch and execute a conditional branch( **Br<0**) is illustrated bellow:

Note: N=0 (positive)

N=1 ( negative)

1 PCout, MARin, Read, Select 4, Add, Zin

2 Zout, PCin, Yin, WMFC

3 MDRout, IRin

4 Branch to 25

25 If N=0 then branch to 1

26 offset Xout, Select y, Add, Zin

27 Zout, PCin, End.

H.W= Br > 0