**Solve hazard:
Structural hazard**

Fix with separate instruction and data memory

1-Reading data from memory

2-Reading instruction from memory

**Data hazard**

* fix data hazard by **waiting** – stall – but impacts CPU
* Fix data hazards by forwarding results as soon as they are available to where they are needed .

**control hazard**

A control hazard, also known as a **branch hazard** , occurs when the pipeline makes the wrong decision on a branch prediction and therefore brings instructions into the pipeline that must subsequently be discarded.

**Fix branch hazard**

dealing with conditional branches:

• Multiple streams

• Prefetch branch target

• Loop buffer

• Branch prediction

• Delayed branch